P-103

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Print Figure: 1

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ELECTRONIC STILL CAMERA

The invention is a hand-held, portable digital camera with a replaceable memory that is battery operated and which can be used with conventional camera accessories and a variety of image sensors to obtain a high quality digital image. In the prior art, images typically are recorded by either film photography or by still video imaging systems. Both these types of imaging systems have certain inherent disadvantages if used in a remote environment where real-time processing is desired. It would, therefore, be advantageous to have a high quality digital imaging system that facilitates real-time analysis by eliminating the necessity of converting or processing the image before computer analysis could be conducted while also producing a high quality image.

The invention comprises a digital electronic camera that provides more than 1,000,000 pixels of resolution. The camera includes a charge-coupled device (CCD) array mounted in a slightly modified commercial camera body. Images are stored in a hard drive disk, or on an alternative storage device, which is removable and replaceable to permit image storage that is limited only by the number of available hard disks. Unlike film, hard disks can be reused if so desired to record over an improperly recorded image. This can be useful in a double-exposure situation, or other operator or camera malfunction. In addition, the invention permits direct transmission of the image, either from the hard disk, or directly from the image sensed by the charge-coupled device array, to a remote location. Photons received through the aperture of the camera are converted into analog signals by the CCD. The operation of the CCD is controlled by a timing generator, which receives signals that indicate when the shutter release button has been pushed, when the shutter opens and when the shutter closes. Timing signals to the CCD are provided by a novel level shifting circuit. The aperture and exposure are controlled by conventional camera settings. The electronic camera is programmable and can include programmable read-out functions, such as anti-blooming, multi-pinned phase, and other advantageous features. The output analog signal from the CCD is amplified and processed in a correlated double sampler to remove noise. A sample and hold circuit further conditions the analog signal for use by the analog-to-digital (A/D) converter. Only certain bits of the A/D converter are used to guarantee accuracy. The digitized signal from the A/D converter is temporarily stored in a memory buffer before it is loaded into the removable permanent memory.

Novelty exists in circuits which permit recording of high quality digital images in real time by means of a hand-held electronic camera.

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ELECTRONIC STILL CAMERA

BACKGROUND OF THE INVENTION

This application relates generally to equipment for taking and storing still images. More particularly, the invention relates to an electronic camera capable of storing the images in digital form or transmitting the images to another location for "real-time" analysis or viewing. Still more particularly, the invention relates to a hand-held, portable digital camera with a replaceable memory that is battery operated and which can be used with conventional camera accessories and a variety of image sensors to obtain a high quality digital image.

In the prior art, images typically are recorded by either film photography or by still video imaging systems. These types of imaging systems have certain inherent disadvantages if used in a remote environment where real-time processing is desired.

Film photographs can result in very high quality imaging, but the images so recorded cannot be readily transmitted to a remote location. In certain applications, such as space flight and satellite reconnaissance, the use of photographic film to record images

is of limited practicality because it is necessary to retrieve the film before the image can be processed. Because of the length of time involved for completion of the mission, the images recorded by film are used primarily for historical purposes. Real-time analysis, quite obviously, is impossible.

Yet another problem with photographic film is that it can only be used, or exposed, once. Thus, if an error occurs during the taking of a picture with photographic film, the film cannot be reused. Common errors are double exposure, out-of-focus images, improper framing of images, and the like.

In addition, once the film is retrieved and processed, it is difficult to analyze the photographs without first digitizing the photographs to permit the use of computer analysis techniques. Computer analysis techniques are commonly used to process the image, restore or reconstruct a portion or all of an image, and the like. Unfortunately, before computer analysis of the images can begin, the images must be converted to an acceptable format for processing. The standard signal used for computer analysis is a digital signal. Consequently, the photographs must be converted to a digital signal (or digitized) before computer analysis can begin. For these and other reasons, where it is desirable to receive and process "real-time" images recorded at a remote location, the use of photographic film is not a viable alternative.

The second type of imaging is electronic video imaging, such as is done with the various commercial "camcorders" and still video cameras on the market. The electronic imaging in these systems comprises analog video imaging that can be electronically

transmitted to remote locations, but which fails to produce a high quality image with acceptable resolution. A still image is obtained by "freezing" the image. The resolution of the "frozen" analog image is poor, thus resulting in low quality pictures.

In addition to the problem of poor resolution, it is difficult to conduct computer analysis on the analog image signals. Before the computer analysis can begin, the analog video signal must be converted to a digital signal. Thus, while the analog video images can be transmitted to a remote location, there is an inherent time delay required for digital conversion. This time delay prevents "real-time" use of the analog image for many applications.

It would be advantageous to develop a high quality digital imaging system that facilitates real-time analysis by eliminating the necessity of converting or processing the image before computer analysis could be conducted while also producing a high quality image. There have been some attempts to develop a digital imaging system. An example of one such system is found in U.K. Patent Application 2,089,169A. The system described is a bulky unit that produces an image with a maximum pixel resolution of 100 x 100 (10,000 pixels of resolution), which is below the quality of a conventional Camcorder. Thus, despite the readily apparent advantages of a digital imaging system, no one to date has developed a digital imaging system that can obtain an image of acceptable quality.

SUMMARY OF INVENTION

The invention constructed in accordance with the preferred embodiment comprises a digital electronic camera that provides more than 1,000,000 pixels of resolution. The camera includes a charge-coupled device ("CCD") array preferably mounted in a slightly modified commercial camera body. The CCD may comprise a 1K x 1K monochrome image sensor, a 2K x 2K monochrome image sensor, a 1K x 1K color image sensor, or any other suitable sensor. Images preferably are stored in a hard drive disk, or on an alternative storage device, which preferably is removable and replaceable to permit image storage that is limited only by the number of available hard disks. Unlike film, hard disks can be reused if so desired to record over an improperly recorded image. This can be useful in a double-exposure situation, or other operator or camera malfunction. In addition, the invention permits direct transmission of the image, either from the hard disk, or directly from the image sensed by the charge-coupled device array, to a remote location.

Because the electronic camera of the preferred embodiment is housed in a conventional-sized camera body, the camera is handheld and portable and preferably operates off of battery power. The system electronics are housed either in the camera body, or in a small electronics box that preferably is removably attached to the bottom of the camera body. A cable connects between the electronics box and the camera to permit the camera and box to be physically separated. Moreover, the camera includes a

conventional input/output data port through which data can be transmitted by a user, for controlling the camera, sending or receiving data to or from the camera, or a variety of other functions.

In addition, because the camera body comprises a conventional off-the-shelf product that has been slightly modified to house the charge coupled device ("CCD"), conventional camera accessories can be used for the optical system. The camera of the preferred embodiment, therefore, can be used in conjunction with conventional camera accessories, including telephoto lenses, wide-angle lenses, flash units, and the like. In addition, the camera preferably includes auto-focusing capabilities, automatic exposure and aperture capabilities and other functional capabilities that commonly are found in conventional off-the-shelve cameras.

The photons received through the aperture of the camera are converted into analog signals by the CCD. The operation of the CCD is controlled by the Timing Generator, which receives signals that indicate when the shutter release button has been pushed, when the shutter opens and when the shutter closes. Timing signals to the CCD is provided by a novel Level Shifting Circuit. The aperture and exposure preferably are controlled by conventional camera settings. The electronic camera preferably is programmable and can include programmable read-out functions, such as anti-blooming, multi-pinned phase (MPP), and other advantageous features. The output analog signal from the CCD is amplified and processed in a correlated double sampler ("CDS") to remove noise. A Sample and Hold Circuit further conditions the analog signal for use

by an Analog to Digital Converter ("A/D"). Only certain bits of the Analog to Digital Converter are used to guarantee accuracy. The digitized signal from the Analog to Digital Converter is temporarily stored in a Memory Buffer, before it is loaded into the removable permanent memory.

The camera also preferably is programmable to enable the electronic still camera ("ESC") to support a wide variety of sensors, sensor readout strategies and system component functions, all of which can be correlated with the recorded image, and stored with the digitized image signal in the removable permanent memory. The camera also includes a high speed data output port to permit high speed transmission for near real-time image transfer to a remote location.

The electronic camera preferably includes hardware and software to minimize power consumption to preserve operating power for long missions or when the camera is used in remote locations. These and other advantages of the invention will become apparent to one skilled in the art on reading the following Detailed Description.

BRIEF DESCRIPTION OF THE DRAWINGS

For a detailed description of the preferred embodiment of the invention, reference will be made now to the accompanying drawings, wherein:

FIG. 1 is a functional block diagram of the preferred embodiment of the invention including the electronic still camera, playback downlink unit and ground station;

FIG. 2 is a detailed functional block diagram of the preferred embodiment of the electronic still camera;

FIG. 3 is a rear view of the electronic still camera constructed in accordance with the preferred embodiment;

FIG. 4 is a side view of the camera shown in FIG. 3;

FIG. 5 is a functional block diagram of the Imager Signal Chain of FIG. 2;

FIG. 6 is a graphical illustration comparing quantum efficiencies obtainable through various image recording devices;

FIG. 7 depicts the output signal waveform of the circuits comprising the Imager Signal Chain of FIG. 6;

FIG. 8 is a functional block diagram of the Timing Generator and Level Shifters of FIG. 2;

FIGS. 9A-9D are timing waveforms illustrating the operation of the Image Pickup Device of FIG. 2;

FIG. 10 is a flow chart depicting programmability of the electronic still camera of FIG. 2;

FIGS. 11A-11B is a flow chart illustrating the operation of the microcomputer of FIG. 2;

FIG. 12 is a schematic illustration of a voltage regulator that forms part of the Power Supply shown in FIG. 2;

FIGS. 13A-B depict the printed circuit boards that comprise the electronic still camera in the preferred embodiment;

FIGS. 14A-B are a circuit schematic illustration of the CCD Circuit shown in FIGS. 2 and 13;

FIG. 15 illustrates the circuits that comprise the Analog PCB, shown in FIG. 13;

FIGS. 16A-B are a circuit schematic illustration of the Analog Circuit of FIG. 15;

FIG. 17 is a circuit schematic illustration of the Camera Interface Circuit depicted in FIG. 15;

FIGS. 18A-C are a circuit schematic illustration of the Buffer Memory Circuit shown in FIGS. 2 and 13;

FIG. 19 illustrates the circuits that comprise the DIGIT 1 PCB of FIG. 13;

FIGS. 20A-B are a circuit schematic illustration of the Microcomputer Circuit of FIG. 19;

FIGS. 21A-B are a circuit schematic illustration of the Hard Disk Interface Circuit of FIG. 19;

FIG. 22 is a circuit schematic illustration of the Input/Output Port Circuit of FIG. 19;

FIG. 23 illustrates the circuits that comprise the DIGIT 2 PCB of FIG. 13;

FIG. 24 is a circuit schematic illustration of the SAM Digital Circuit of FIG. 23;

FIG. 25 is a circuit schematic illustration of the Downlink Interface Circuit of FIG. 23;

FIG. 26 is a circuit schematic illustration of the User Data Interface Circuit of FIG. 23;

FIG. 27 is a circuit schematic illustration of the LCD circuit shown in FIG. 13;

FIG. 28 shows the circuits that comprise the Power Supply PCB of FIGS. 2 and 13;

FIG. 29 is a circuit schematic illustration of the Power Supply Circuit of FIG. 28;

FIG. 30 is a circuit schematic illustration of the Battery Low Circuit of FIG. 28;

FIG. 31 shows an operations time line for the electronic still camera of FIG. 1;

FIG. 32 is a flow chart depicting the signals shared with the Camera Body of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

This description will begin with a discussion of the entire Electronic Still Camera ("ESC") System, as currently envisioned by NASA, including the Camera (which is alternatively referred to herein as the "ESC"), the Playback/Downlink Unit, and the Ground Station. After gaining a perspective of the invention, the focus will turn primarily to the functional elements of the Camera and its overall operation. The description will conclude with a discussion on the circuitry used to construct the preferred embodiment of the Camera.

I. SYSTEM OVERVIEW

Referring now to Figure 1, the NASA Electronic Still Camera System preferably comprises three basic units, with the primary focus being on the Camera in this application. The three units preferably are the Camera (also alternatively referred to herein as the Electronic Still Camera, or "ESC"), the Shuttle Playback Downlink Unit and the Ground Station. As a general overview, the user operates the Camera as a regular 35mm camera 5 but with a removable hard drive 80 functioning as the image storage media instead of a film cartridge. The Camera has a Standard Data Input 120 that can be used as a data input in conjunction with the image recording and storing to correlate the image with other external data. For example, as shown in Figure 1, NASA currently plans to use Latitude and Longitude Locator (L3) data for each image taken when the L3 device is attached. Thus, according to the preferred embodiment, an L3 unit connects to the Standard Data Port 120 (Figure 2) to provide the L3 signals to the ESC system for matching with the recorded image. The ESC then correlates the L3 signal that is automatically obtained when each image is taken with the corresponding digitized image, so that the geographic location of each image is stored together with the image signals in the removable permanent memory. One skilled in the art will realize that a myriad of other data inputs could be used in place of or in addition to the L3 to provide additional correlation of other sensed parameters.

The Camera preferably uses a custom "made for NASA" Nikon F4 for its optical imaging system. Obviously, other conventional cameras could be used in place of the Nikon F4. As shown in Figure 1, the Camera has the capability to downlink directly through the space vessel's downlink system in a variety of modes. The Playback Downlink Unit receives the removable hard drive from the camera, displays images on the space vessel's onboard monitor, processes the images and downlinks the images using conventional transmission techniques.

The Ground Station receives the image data, either during flight or post flight, archives the images, processes the images, and supplies the data in a variety of forms for use and analysis. These forms include digital data, image files, hard copy output and CRT viewing of the images.

While the foregoing description focuses on the use of the camera aboard a space vessel, it should be understand that the Camera constructed in accordance with the preferred embodiment can and is intended to be used in numerous other applications. Thus, it should be understand by anyone who reads this description that the following teachings cover any and all applications for which this Camera can be used.

II. FUNCTIONAL DESCRIPTION OF THE ELECTRONIC STILL CAMERA

Referring now to Figures 2-4, the electronic still camera ("ESC") constructed in accordance with the preferred embodiment comprises two physical elements -- the Camera Body 20 and an associated Electronics Box 15. The circuitry associated with the Image

Pickup Device 30, including the Preamp Circuitry 35, the Correlated Double Sampler 40, the Sample and Hold circuitry 45, the Analog-to-Digital Converter 60 line drivers 61, level shifter 90, and line receivers 74 are housed in the Camera Body 20. The remaining circuit elements of the ESC depicted in the functional block diagram of Figure 2 reside in the Electronics Box 15. The Electronics Box 15 may be physically attached to the Camera Body 20 as shown in Figures 3 and 4, or may be detached from the Camera Body 20 and electrically connected thereto by suitable high speed electrical cables 63, 64.

Referring now to Figure 2, the invention constructed in accordance with the preferred embodiment generally comprises an Optical Imaging System 17 used with the Camera Body 20 to receive photons to obtain an optical image, an Imager Signal Chain 50 for converting the photons to an electrical signal representative of the image, a Timing Generator 75, a Microcomputer 100, a Permanent Memory 80 for storing the signals representative of the image, Input and Output Circuitry 120, 130 (output only), and a Power Supply 85.

A detailed description of each of these functional components follows.

A. OPTICAL IMAGING SYSTEM 17

Referring now to Figures 2-4, the Optical Imaging System 17 preferably comprises as a conventional image focusing device, including an optical lens, a fiberscope, a telescope, a microscope or any other instrument that can be adapted to create an optical image. Essentially, the Optical Imaging System 17 is an apparatus for bringing the incoming photons to the Camera Body 20. It may be used to determine the spectral

response of the system by allowing only certain wavelengths of light to pass, such as, for example, only infrared light waves. This is useful for many applications such as for multispectral imaging or to make it possible to use the metering system of the Camera Body 20 to operate as a conventional film camera with a built in metering system. The Optical Imaging System 17 is one of the system components which determine the overall resolution of the system. The Optical Imaging System 17 may be automatic to allow for autofocus and autoaperature settings thus making the system manual or automatic.

B. *CAMERA BODY 20*

Referring still to Figures 2-4, the Camera Body 20 is an electro-mechanical-optical assembly that houses the system components. In the preferred embodiment, the camera body comprises an off-the-shelf camera that has been slightly modified to physically receive the Image Pickup Device 30 ("CCD") and to provide for electrical input signals and output signals. In the preferred embodiment, a Nikon F4 is used. The Camera Body 20 adapts the Optical System 17 to the Image Pickup Device 30, while also providing some interface with the Operator of the system. The Camera Body 20 preferably includes a means for allowing the Operator to see the image that the Optical System 10 is transmitting, through the use of a viewfinder 18 or an adapted video camera (not shown). In addition, the Camera Body 20 permits the Operator to control the system, by regulating the normal settings of an SLR Camera such as shutter speed setting 22, aperture setting, exposure mode, exposure compensation, ASA setting 23, and the like.

In the preferred embodiment, the conventional Camera Body is modified to alter or remove the conventional film rails internal to the Camera Body to define a compartment for receiving the Image Pickup Device 30 in a position that is in close proximity to the shutter. A second modification is that the viewfinder 18 is modified to conform to the shape of the Image Pickup Device 30 to assist the Operator in framing the picture. A final modification is that the shutter release button (not shown) is not directly connected to the shutter, but instead connects to the Timing Generator 75 and Microcomputer 100, which control the opening of the shutter. Just as in a conventional camera, however, the images received by the camera are determined by the characteristics of the Imaging System 17 and the Operator controls (whether they are automatic, as in an SLR mode, or are manual).

By using a Camera Body 20 that includes a shutter, full frame image sensors may be used. As a result of using a full frame image sensor, higher resolution images may be obtained due to the fact that the entire image sensor is used for imaging.

As noted above, the viewfinder 18 preferably is masked off to show only the portion of the field of view which is imaged. By shaping the viewfinder to correspond to the shape of the Image Pickup Device 30, the Operator can determine accurately the image that will be received by the Image Pickup Device 30. Moreover, using large format imager sensors facilitates the use of a viewfinder whereas small format imager sensors make framing of the image difficult.

The controls, indicators and displays allow the Operator to interact with the camera. Referring now to Figure 3, the On Off Switch 24 applies power to the camera. A PWR LED 26 lights when the power is turned on. The camera uses a programmable Mode Switch 27. The function of the Mode Switch 27 can be changed to support a variety of operating scenarios. In the preferred embodiment, the ESC has a four position Mode Switch 27 which determines how the images will be stored and when they will be transmitted. These operating modes preferably are: (1) take picture, store on disc; (2) take picture, store on disc, downlink image; (3) take picture, store on disc, downlink image, do not move to next frame count; and (4) downlink entire disc. The Display 28 preferably comprises an LCD display that provides the Operator with information on the status of the camera. The LCD display 28 also is programmable to enable the ESC to give indications for particular applications. Typically the LCD display 28 is used to show which frame number the camera is on, whether the battery is low, malfunction identification and current operation identification. The Reset Buttons 29 are used to reset the system if there is a malfunction or if the User would like to retake an image without advancing to the next location in memory.

The interfacing between the external system circuitry and the Nikon F4 must allow for the timing and character of the camera. Also, the other system components must be able to communicate with the Camera to make the system operate in an organized fashion. An example time line for ESC operations and signals passed between the components are shown in Figures 31 and 32.

Referring now to Figure 3, 31 and 32, the ESC is activated by pressing the shutter release button (not shown). When the shutter release 72 is activated, the Microcomputer 100 (Figure 2) receives a pulse (N1) and activates the Timing Generator 75, which turns on the ESC circuits in preparation for opening the shutter; the shutter, however, is not opened immediately. During this period, the Image Pickup Device 30 dumps its contents, or resets, in preparation for receiving the photons through the operation of the camera. When all circuits are ready, the Timing Generator 75 generates a pulse (N2) that is transmitted to the Camera Body 20 to fire the shutter. The delay between the Image Pickup dump and the time when the shutter fires is referred to as the Shutter Delay in Figure 31. The length of time that the shutter is left open is dictated by the settings on the Camera (exposure setting). When the shutter closes, the Camera circuitry transmits a signal (N3) to the Timing Generator 75, which causes the Image Pickup Device 30 to transmit its contents to a Memory Buffer 65, via the Imager Signal Chain Circuitry 50.

C. IMAGER SIGNAL CHAIN CIRCUITRY 50

Referring now to Figure 2 and 5, the portion of the system starting with the Image Pickup Device 30 (or Image Sensor) and ending with the Memory Buffer 65 also is referred to as the Imager Signal Chain 50. The Imager Signal Chain 50, therefore, is responsible for receiving incoming photons from the Optical Imaging System 17 and Camera Body 20 and converting these photons into electrical signals that can be used by the remaining system circuitry. One of the system requirements is that the Imager Signal Chain 50 must maintain the integrity of the imaging while processing the electrical signal.

1. Image Pickup Device 30

Referring again to Figure 2, the Image Pickup Device 30 (also referred alternatively to herein as "Image Sensor") is the system component which interfaces the optical subsystem to the electrical subsystem for the applications required of the system. In the preferred embodiment, for example, it comprises a Charged Coupled Device (CCD). As will be realized by one skilled in the art, other image pickup devices may be used without departing from the principles of this invention.

The Image Pickup Device 30 receives the incoming photons and converts them into electrical signals which can be used by the circuit components of the ESC. The Image Pickup Device 30 reads the image produced in a way that a high fidelity interpretation of the image can be derived from reading the device.

The Image Pickup Device 30 can comprise a Loral 1024L 1K x 1K monochrome CCD, a Loral 2048S 2K x 2K monochrome CCD, a Loral 2048S 1K x 1K color CCD, or any other type of photon conversion device. Due to the programmability of the camera, a variety of image sensors and sensor readout strategies can be implemented. If the Image Pickup Device 30 is one of the Loral CCD's it can be operated in the multi pinned phase ("MPP"), *see* US Patent No. 4,963,952, issued to J.R. Janesick, the teachings of which are incorporated by reference herein, or in the Clocked Recombination Antiblooming mode ("CRAB").

The MPP mode allows for very good dark current suppression at room temperatures and the CRAB mode suppresses blooming without decreasing the sensitivity

of the CCD or reducing the fill factor of the CCD. As will be understood by one skilled in the art, the fill factor relates to the amount of surface area that is active on the face of the Image Pickup Device 30. Most Imager Sensors 30 are manufactured with a cover glass to protect the front surface of the Sensor. It has been discovered that by removing the glass and employing other means to protect the Image Pickup Device 30, optical noise in the form of reflections can be reduced significantly. Instead of using the glass protective plate, in the preferred embodiment the wiring is secured to the Image Pickup Device 30 by a suitable optical epoxy so that the CCD will be maintained in position and will not be damaged.

By choosing an Image Pickup Device 30 with a large pixel size the optical characteristics of the ESC System are not stressed. This results in a system which is not limited in resolution by the optics. The use of smaller pixels makes it difficult to produce a satisfactory modulation transfer function ("MTF") at maximum resolution due to the optical limitations. The Quantum Efficiency of Imager Sensors usable in the preferred embodiment of the ESC can be shown to be superior to film or the human eye. *See* Figure 6.

The Image Pickup Device 30 requires a large number of different voltages levels for its operation. By using local regulated power supplies 32 for the Imager Signal Chain, the induced noise from the main power supply can be reduced. The power supplies 32 are also adjustable ("programmable") so that the CCD can be optimized for specific parameters. Some of the parameters which may be changed by adjusting these

levels are the amount of antiblooming, full well capacity, radiation hardness, spurious charge reduction and output amplifier gain.

2. *Preamp Circuitry 35*

Referring still to Figure 2, the Preamp Circuitry 35 comprises an electronic amplifier. It takes the output signal from the Image Pickup Device 30, buffers the signal and raises the signal level to an acceptable magnitude usable by the rest of the circuit elements. In accordance with the preferred embodiment, conventional circuit amplifiers are used for the Preamp Circuitry 35, as will be discussed in more detail *infra*, in Section III.

3. *Correlated Double Sampler ("CDS") 40*

Referring now to Figures 2 and 5, the Correlated Double Sampler ("CDS") 40 is a circuit with an output that reflects the amplitude of the current pixel being read from the Image Pickup Device 30. The CDS 40 takes in the amplified CCD output from the Preamp Circuit 35 and produces as its output 44 the subtraction of the "live" pixel level and the reset level prior to the live pixel level. By this procedure, correlated noise is eliminated and only the signal caused by the individual pixel is left. If this procedure is done with the right timing, the correlated noise effectively can be subtracted out but, the noncorrelated noise remains.

Referring still to Figures 2 and 5, the CDS 40 delays the reset level time by sending the Preamp output to a Circuit with Delay 42. The output of this circuit is fed to one input of a Difference Amplifier 41. The Preamp output signal also connects to a Circuit without Delay 43 and then to the other input of the Difference Amplifier 41. The two inputs to the Difference Amplifier 41 cause the live pixel time to coincide with the delayed reset level at the Difference Amplifier 41. At the end of the live pixel time, the Difference Amplifier 41 outputs the difference of these two signals on output line 44. The combination of the Circuit With Delay 42, the Circuit Without Delay 43 and the Difference Amplifier 41 comprises a Correlated Double Sampling Circuit 40. Some circuits which have been designed to perform a similar function use multiple analog switches or multiple sample and holds. The large transients caused by analog switches combined with the fact that the turn on to turn off ratio is lacking, generally make these types of designs lower performance components. By eliminating analog switches from this circuit, lower noise performance can be achieved due to the elimination of unwanted transients. Implementing this circuit with a delay provides superior results. The Difference Amplifier 41 also functions as a filter to limit the noise bandwidth of the Imager Signal Chain 50. An optimum bandwidth is chosen to limit as much noise as possible but still ensure that the required pixel value can be reached before the Sample and Hold circuit takes its sample. *See* the Imager Signal Chain Signals shown in Figure 7.

4. Sample and Hold Circuit 45

Referring now to Figures 2, 5 and 7, the Sample and Hold Circuit 45 is designed to produce a constant amplitude signal by taking a sample of an incoming signal at an instant in time. It may transform this sample, for example, in magnitude, but its primary function is to hold a version of this time sampled signal constant on its output. The Sample and Hold Circuit 45 receives the output of the CDS 40. At the point in time when the CDS 40 is outputting the desired signal, which represents the pixel value, the Sample and Hold Circuit 45 preferably holds the representative signal for a time duration long enough for the Analog to Digital Converter 60 to perform its conversion.

As shown in Figure 7, the output of the Difference Amplifier 41 is inverted and sampled and held by the Sample and Hold Circuit 45. This is the signal required for the Analog to Digital Converter 60.

5. Analog-to-Digital Converter ("A/D") 60

Referring again to Figures 2 and 5, the Analog to Digital Converter ("A/D") 60 is a circuit which converts an incoming analog signal to a digital signal representative of the amplitude of the analog signal. The A/D 60 receives the output signal from the Sample and Hold Circuit 45 and converts it to a digital signal according to conventional techniques. Digital signals representing the Sample and Hold Circuit's output then are transferred under control from the Timing Generator 75 to the Memory Buffer 65 (described below). Each pixel of the image has its own digital representation after

conversion by the A/D 60. The ESC is unique in that it uses only the higher order bits out of its A/D converter. The ESC uses an A/D which has a larger number of bits, x that is accurate to only a certain number y out of the x bits. The ESC guarantees system accuracy by using only the number of bits y which are accurate. The remaining bits are not used.

Referring now to Figures 2 and 5, the Line Drivers 61 and Receivers 62 preferably comprise RS-422 line drivers to differentially drive the data lines 63, 64 between detachable components of the Camera. By making the Camera into detachable components, versatility is added by allowing the system to be used as a one piece system or multiple piece system. Different lengths of cables attach to the different components for various needs. Thus, according to the preferred embodiment of Figures 2, 3, 4 and 5, the Image Pickup Device 30, CDS 40, Sample and Hold Circuit 45, A/D 60 and Line Driver 61 are all housed in the Camera Body 20. The Line Receiver 62, Memory Buffer 65, Timing Generator 75, Microcomputer 100, Power Source 70, Input/Output Connections all are housed in a separate Electronics Box 15. Detachable cables 63, 64 connects the circuitry of the Body 20 to the circuitry of the Electronics Box 15.

6. Memory Buffer 65

Referring now to Figures 2 and 5, the Memory Buffer 65 preferably comprises a circuit that stores the digital representation of the image prior to being used by the Microcomputer circuit 100. The Timing Generator 75 produces signals that cause the Memory Buffer 65 to receive the data from the A/D 60 at appropriate times.

Thus, the Memory Buffer 65 receives signals from the Timing Generator 75 enabling it to receive the data from the A/D 60 by way of the Line Driver 61 and Line Receiver 62. An image or multiple images then are stored in the Memory Buffer 65. The Memory Buffer 65 can then be read out under control of the Microcomputer 100 by way of the Buffer 66 for a variety of reasons, such as to read into Permanent Memory 80, or to send to another part of the circuit such as the High Speed Data Port 130 for immediate transmission, or to be manipulated by the Microcomputer Circuit 100 for data compression, analysis, etc. The Memory Buffer 65 can be made to support various sizes of memory integrated circuits ("ICs"). By doing this, Image Pickup Devices 30 with higher or lower resolution can be used which produce different amounts of total data per image. The advantage of writing the data to a Memory Buffer 65 before it is sent to the Permanent Memory 80 is that the Image Pickup Device 30 can be read out at a constant rate. Many Permanent Memory 80 systems have wait states which could cause delays and vary the characteristics of the pixels being readout.

7. *Level Shifters 90*

Referring now to Figures 2 and 8, the Level Shifters 90 are circuits that change the voltage levels of their inputs to different voltage levels appropriate for activating and running the Image Pickup Device 30. If the Image Pickup Device 30 is a CCD in accordance with the preferred embodiment, several voltage levels are necessary for operation. The Level Shifters 90 take the digital logic level voltage input signals and

convert them to the different voltage levels as required for operating the Image Pickup Device 30. The Level Shifters 90 are critical to the performance of this kind of system and great care needs to be taken on how these are used.

The turn on and turn off time of the Level Shifter circuits 90 must be very short. Slower turn on and turn off designs result in unusable circuit characteristics. The design does not use negative feedback. Leaving out negative feedback ensures that large current transitions during a voltage level hold period will not occur. The preferred design, shown in Figure 8, also has a very low power consumption while idle, which is important to a camera of this type when it is powered from battery power. The RC filter on the output of each Level Shifter allows tailoring of the rise and fall time of the signal. Too fast of a rise time can cause spurious charge in the CCD, too slow a rise timed can cause insufficient charge transfer throughout the CCD.

D. PERMANENT MEMORY 80

Referring again to Figure 2, Permanent Memory 80 comprises a data storage system which stores data even after system power has been turned off. The Permanent Memory 80 stores permanent digital versions of the images obtained by the Imager Signal Chain 50. The Permanent Memory 80 preferably is removable so that other memory disks or cartridges can be substituted for the present memory disk or cartridge when it is full. In this manner, the number of images which can be stored is limited only by the number of available memory devices. The permanent memory also preferably performs special functions, such as storing the programs for the Microcomputer Circuit 100, and

loading them after power up, powering down to save system energy and saving special data from devices such as date and time clocks or data from the Data Port 120.

The Permanent Memory 80 is analogous to film cartridges in a typical film camera. While various memory devices could be used, such as CD disks, floppy disks, and the like, a Hard Drive preferably is used as the Permanent Memory 80 because it includes the following advantages: (1) it has a high bit density; (2) it can include power down modes to save battery power; (3) it is nonvolatile, so it retains its data after power is taken away; and (4) it has a high read/write speed. The Hard Drive can include a DISK indicator that is lit to notify the User when a disk read or write is being performed. By using Removable Hard Drives, different programs can be loaded on different Drives to perform varying functions. For example, one Drive could have a program that brings in data from a Latitude Longitude Locating (L3) device and that stores data with each image; another Drive could have programs which allow operation of the camera with different time delays. Similarly, the Hard Drive could provide special indications on the LCD Display 28 for special applications or could downlink images without storing them on a disk. As one skilled in the art will realize, the various programs that could be stored on the Hard Drive for use in the ESC System are virtually unlimited.

E. TIMING GENERATOR 75

Referring to Figures 2 and 10, the two processing circuits which have control over the camera at different times in its operation are the Timing Generator 75 and the Microcomputer 100. The relationship between the Timing Generator 75, the Microcomputer 100 and the rest of the Camera is illustrated in the programming flow chart of FIG 10. During the Image Pickup Device 30 readout period, the Timing Generator 75 is active. The rest of the time the Timing Generator 75 waits for activation from the Microcomputer 100.

Referring now to Figures 2 and 8, the Timing Generator 75 and its associated circuits are shown in accordance with the preferred embodiment. The associated circuits include a Synchronizer 77, a Line Receiver 73, a Line Driver 76 and an Oscillator 71. The Line Receiver 73 connects electrically to the Camera Interface Circuitry 25, from which it receives output signals indicating camera operation. The output of the Line Receiver 73, in turn, connects to the Synchronizer 77, which also receives input signals from the Microcomputer 100. The output of the Synchronizer 77 connects to the Programmable Timing Generator 75 and the output of the Timing Generator 75 connects to a Line Driver 76. The Line Driver 76 electrically connects to a Line Receiver 74 and then to the Level Shifter 89 via a cable 63 to permit the Camera Body 20 to be detached from the Electronics Box 15 that houses the Timing Generator 75 and Microcomputer 100.

Initially, signals are received from the Microcomputer 100 which initiate the Image Sensor 30 readout sequence of the Timing Generator 75. These signals are synchronized by the Synchronizer 77. Signals also are received from the Camera Interface 75 through the Line Receiver 73 and Synchronizer 77. These signals allow the Timing Generator 75 to know the status of the Camera Body 20 such as when the shutter has been opened (pulse N1 in Figures 1, 30 and 31) and when it has closed (pulse N3 in Figures 1, 30 and 31). The synchronizer insures that the Microcomputer's controlling signals do not violate the set up or hold time of the Timing Generator's inputs. The Timing Generator 75 controls the Image Pickup Device 30 and the Camera Body 20 by way of the Line Driver 76 and Line Receiver 74. As noted, the Line Driver 76 and Line Receiver 74 are included to allow the system to be produced in detachable parts. The timing must be level shifted by the Level Shifting Circuits 90 when different voltage levels are required.

The Timing Generator 75 preferably comprises a Programmable Logic Device, such as the Altera EPS-448 Stand Alone Microsequencer (SAM). By using a device of this type, versatility is added to the system by enabling the Timing Generator 75 to be reprogrammed for a variety of sensors and sensor readout strategies. Knowledge of how to program the SAM is provided by the manufacturer, ALTERA. Two examples of programs usable for a system of this type are included in the Appendix, one for MPP operation and one for CRAB operation. Again, due to the programmability of this design, these examples are only two of many possibilities. The utility of a programmable camera allows changes which are only limited by the imagination of the programmer. The

example programs for the SAM implement the timing waveforms of FIGS. 9A-9D for the Loral family of CCDs.

Once activation is received from the Microcomputer 100 the SAM executes a Charge Dumping Sequence, as shown in the timing waveform analysis of FIG 9A. The Charge Dumping Sequence preferably is repeated several times to evacuate the CCD of accumulated charge due to thermal energy. At the completion of the Charge Dump period, the shutter is opened by SAM control and the Light Integration period begins. This is illustrated in Figure 9B for MPP operation and Figure 9C for CRAB operation. After the SAM is notified that the shutter has been closed, the CCD then is readout and the resulting data is stored in the Memory Buffer 65, as shown in FIG 9D. Upon completion of this operation, control signals let the Microcomputer 100 know that the sequence has been completed and that the digitized image now resides in the Memory Buffer 65.

F. MICROCOMPUTER 100

The Microcomputer is a circuit that can be programmed to produce a variety of functions and operations. It can use an operating system to facilitate the interfacing to system peripherals and it can communicate with the outside world and make preprogrammed decisions to determine how to control the ESC System. Referring now to Figure 2, the Microcomputer 100 receives input signals from the Control Circuit 110, Permanent Memory 80, Power Supply 85, Standard Data Port 120, Camera Body 20, Timing Generator 75 and Memory Buffer 65. The Microcomputer 100 also transmits

output signals to the Permanent Memory 80, Timing Generator 75, Camera Body 20, High Speed Data Port 130, Standard Data Port 120, Indicator/Display 95 and Power Supply 85. By a combination of firmware and software programs the Microcomputer 100 orchestrates the operation of the ESC, determining what will be done, how it will be done, and when it will be done. The Microcomputer 100 preferably is programmable so that an endless number of programs can be loaded and run which control the system and its peripherals for a variety of applications and needs.

In the preferred embodiment, the firmware is located in the BIOS (Basic Input Output System) and the software is loaded from the Permanent Memory as described *supra* in section III(C). The Microcomputer 100 communicates with the Camera Body 20 to execute image taking sequences. The Timing Generator 75 works in cooperation with the Microcomputer 100 and has the responsibility of sending the images into the Memory Buffer 65. From the Memory Buffer 65, the Microcomputer 100 can reroute the data to any and all elements under its control, including the Permanent Memory 80, High Speed Data Port 130, and Standard Data Port 120. The Microcomputer 100 controls the Power Supply 85 and can activate and deactivate it for different power supply needs. It also receives signals from the operator through the Control Circuitry 110 to help it make decisions as to how to operate and send signals to indicators and displays to inform the Operator regarding system operation. As noted above in Section II(A)(2), one of the controls can be a multiposition mode switch 27 (Figure 3) which can be selected by the Operator to choose different programmed functions.

The Microcomputer 100 preferably comprises a DOS system. In the preferred embodiment, a Wildcard 88 is used. By using a standard DOS system, the programming is within the skill of individuals familiar with writing DOS Personal Computer Programs. In addition, the programs preferably are a combination of 'C' and Assembler languages. An example of how the Microcomputer circuit 100 can be programmed will illustrate one of the many possible programs which could be utilized. This example shows that the Program Controlled Functions of FIG 10 are programmed. One skilled in the art will realize that this example is merely illustrative and that the number of possible programming scenarios is limited only by the programmer's imagination.

Referring now to FIG 11A and 11B, an example program is illustrated which can operate this camera. The actual program which implements this flow chart can be found in the attached Appendix. The programmable mode function 27 (Figure 3) is used in this example to reroute the program's flow. For example, as shown in Figure 3, Mode 3 is a downlink function. According to the preferred embodiment of FIG 11A, Mode 3 is checked to determine whether to downlink images or not. The four modes implemented by this particular program are: Mode 1 = Take Picture and Store on Disk, Mode 2 = Take Picture, Store on Disk, Downlink, Mode 3 = Downlink all selected Images, Mode 4 = 10 Second Self Timer version of Mode 1. *See* Figure 3. The downlink function is accomplished through the High Speed Data Port 130, shown in FIG 2. In accordance with the preferred embodiment, the Permanent Memory 80 comprises a disk drive.

To be able to write a program to control the camera's functions the programmer needs to know some specific information about the camera hardware. The manner in which to use this information is shown in the example program in the Appendix. First, since the system is a DOS based computer, an AUTOEXEC. BAT can be used to start the program execution whenever the system is "booted" or turned on. In the example, the program 'xtclock.com' is employed to set the Microcomputer's date and time to correspond to the date and time of the Date and Time Clock 104 that preferably forms part of the Microcomputer Circuit 100. *See* FIG 2. This can be a No-Slot Clock, such as is made by Dallas Semiconductor. The program 'xtclock.com' is commercially available software for this device. The next command, 'd:' changes the default disk drive to d:. In this example the Permanent Memory 80 preferably comprises a Prairie Tek 240 Hard Drive. This assumes that the Permanent Memory is a Hard Disk Drive with two partitions, c: and d:. The program 'pwrtest.exe' is then executed to set up the Hard Drive to go into a low power mode if it has not been accessed within a preprogrammed period of time. The example program 'pwrtest.exe' illustrates one way of doing this. The information from the manufacturer, Prairie Tek is used to enable a programmer to write programs of this type. The program 'zwait.exe' is then executed to set up the Wildcard 88 for 10 Mhz operation and the minimum amount of wait states. The example shows one implementation of this operation. The information which enables a programmer to program the Wildcard is available from the Manufacturer, Intel. The last program to be

executed is escdtt2.exe. This program implements the rest of the flowchart of figure 11A and 11B.

The main module is written in 'C'. It calls up the other modules (functions) which are written in Assembler. To program the camera the addresses of the components under program control must be known. These are:

Inputs to Microcomputer

03E8h Bits 0 through 7 - Data input to Microcomputer from Memory Buffer.

03E9h Bits 0 - READY - Relates when SAM has completed the imaging cycle.
Bit 1 - MO - Mode 0 active.
Bit 2 - TAKPIC - Relates that User has depressed the shutter release button.
Bit 3 - M3 - Mode 3 active.
Bit 4 - M2 - Mode 2 active.
Bit 5 - M1 - Mode 1 active.
Bit 6 - L3 - Relates that a User data input or output device is hooked up to the Standard Data Port.

Outputs from Microcomputer

03E8h Bits 0 through 7 - Down Link Port Data - writing data to this address results in it being sent out the High Speed Data Port.

03E9h Bit 0 - INCC - increments memory counter of Memory Buffer when data is read from Memory Buffer.
Bit 1 - RESETC - resets memory counter of Memory Buffer to beginning of memory address.
Bit 2 - CAMST - transfers control to SAM for image taking sequence.
Bits 3 and 4 high = PWRUP - powers up circuits for picture taking cycle.
Bits 3 and 4 low = PWRDWN - powers down circuits from picture taking cycle.

03EAh Bits 0 through 7 = LCD Display - write two digit BCD numbers to this address to be displayed.

Input and Output

3F8-3FF Standard Data Port is located in the COM1 address space of IBM XT and compatible's convention.

The example program contains Assembler modules which use these I/O Port addresses to accomplish programmable control of the camera in accordance with conventional techniques.

G. INPUT / OUTPUT CIRCUITRY

1. High Speed Data Port 130

Referring again to Figure 2, the High Speed Data Port 130 is an application specific high speed port required to transfer to a remote location the large amounts of data incurred in high resolution electronic imaging. The High Speed Data Port 130 is a nonstandard high speed port reconfigurable to communicate with various transmission rates and schemes such as Shuttle Ku Band Digital Data, Aircraft High Speed Digital Data for DOD purposes, high data rate ground based systems, and high throughput required systems which want the system data at high speed. The High Speed Data Port 130 receives data from the Microcomputer 100 and transmits it to the applicable data interface. It can be formatted to satisfy Operator needs and protocol by changing bit sync identifiers. The system can be made to run at 1.908 MBPS or 9.54 MBPS when implemented with the Wildcard 88 system. These speeds allow it to synchronize with the

Wildcard by using its system clock. The Port can be made to draw very little power when idle by designing in low power states.

2. *Standard Data Port 120*

The Standard Data Port 120 is a digital data input / output system which meets industrial standards and is a relatively easy port with which to interface. It can be used for User Data / Control Input or Data / Control Output. Because the Standard Data Port 120 interfaces to the Microcomputer 100, its function is programmable and unlimited in scope. The Standard Data Port 120 sends and receives data to and from external systems. It also can be used to control the system from an external circuit or computer and it can be used to get information into or out of the system while operating or idle. For example, user data can be stored in the Permanent Memory 80 corresponding to images taken at a certain time. As mentioned previously, the Standard Data Port 120 can be used to bring in data such as Latitude / Longitude Data (L3) (*See* Figure 1) for each image taken. It can interface the system to a wide variety of standard digital peripherals, such as Modems, Printers, Plotters, and the like. It also can allow the Operator to input data into its port and output it at high speed through the High Speed Data Port 130.

If the Standard Data Port 120 is used as COM1 of the IBM XT standard, existing commercially available software packages such as Kermit (for file transfers) or Smart Term (to control the camera from a remote terminal) can be implemented.

3. *Control Circuitry 110*

The Control Circuitry 110 provides a method for the Operator to determine system operation. The Control Circuitry 110 powers up the system or resets the system if necessary or in a situation when the Operator would like to retake an image. The Control Circuitry 110 also can be used to select one of the programmable modes (Mode 1, 2, 3 and 4 on switch 27 in Figure 3) for operation. The programmable modes can be Control selected and software programmable. By doing this a programmed number of operations and characteristics can be activated. Different Permanent Memories 80 can hold different programs making the programmable modes change function depending on which Permanent Memory 80 is in use. Thus, it will be understood by one skilled in the art that the function of the Control Circuitry modes can be changed by simply changing Permanent Memory 80 cartridges or disks.

4. *Indicator/Display 95*

The Indicator / Display 95 are circuits and devices used to provide the operator with information regarding system operation. By viewing the Indicators / Displays 95, the operator can determine the status of the system. The operator can determine when the battery or power source needs attention, how many images have been taken, and what the system is doing, (downlinking, storing data, or communicating to the outside world). Because the Display 28 in the system is programmable through the Microcomputer 100, the indicator also can inform the operator of malfunctions or provide various types of other information.

H. POWER SUPPLY 85

The Power Supply 85 provides the necessary conversion from the Power Source 70 to satisfy the requirements of the rest of the system. The Power Supply 85 receives as an input the power signal from the Power Source 70 and changes this available energy into different voltage levels and current potentials which the circuits require. It can contain special circuits to let the operator know when the Power Source 70 is running low. It also can be under program control from the Microcomputer 100 to perform power management to conserve the Power Source 70.

For example, the analog circuits in the camera can be powered down when a picture taking sequence is completed, if a removable hard drive is used with a programmable low power state, turning off parts of the circuit which are currently not in use. The Power Supply 85 can send signals to the Microcomputer 100 to put it in a reset mode if the power gets too low. By using a variety of power management strategies the camera is designed to operate longer on each battery. All of the circuits of the system are designed with power saving in mind. Parts have been chosen throughout the circuits which will perform the necessary function with the least amount of power. The camera preferably operates off of a 6V Nicad battery. If such a battery is used, and because many of the circuits require 5V, a voltage regulator which has a small input to output drop voltage must be employed. Normal voltage regulators have a drop voltage of about 3V. By using a Power MOSFET transistor in a series pass configuration the drop voltage can be made very low. An example of a design of this type is illustrated in FIG 12. This

particular design would have a drop voltage of only .07V when 1 Amp of current is flowing through the series-pass MOSFET.

The Power Source 70 is the source of energy that powers the camera. This power source preferably is a rechargeable Nicad battery, but also could comprise an AC/DC supply or a DC/DC supply.

III. SYSTEM COMPONENTS

In the following discussion regarding the circuit elements of the electronic still camera ("ESC"), the elements will be discussed based upon their location on each of the printed circuit boards ("PCB's") that are used in the preferred embodiment of the ESC. This is done to assist the person skilled in the art in manufacturing the ESC. It should be understand, however, that the layout of the circuit elements on the circuit boards could be altered by one skilled in the art without departing from the principles of the present invention. Similarly, other circuit elements could be substituted for the elements used in the preferred embodiment without departing from the underlying principle of this invention.

Referring now to Figure 13, a general layout of the ESC System components includes a CCD printed circuit board ("PCB") for converting photons to an electrical analog signal, an Analog PCB receiving and processing the analog image signal, a Memory PCB, two digital PCB's including a DIGIT 1 PCB and a DIGIT 2 PCB, an LCD PCB, and a Power Supply PCB. The Analog PCB and CCD PCB preferably are located

in the Camera Body 20 (FIG. 3), while the remaining printed circuit boards preferably are contained in the Electronics Box 15 (FIG. 3).

A. CCD PCB / CCD CIRCUIT

Referring now to Figures 13A-B and 14A-B, the CCD (Charge Coupled Device) PCB 200, as mentioned, is one of two circuit boards that are mounted in the Camera Body 20. The CCD PCB 200 preferably includes the Image Pickup Device 30 (Figure 2), which preferably is a charge coupled device or "CCD" 210. The CCD PCB 200 also preferably includes the Preamp Circuitry 35, Level Shifters 90 and the Power Supplies 205.

The circuit schematic drawing for the CCD Circuit is shown in Figures 14A and 14B and preferably includes Line Receivers (201, 202), power supplies 205, and the CCD unit 210. Starting in the upper left hand corner of Figure 14A, integrated circuits 201 and 202 preferably comprise RS-422 Differential Line Receivers. These integrated circuits are used for transmitting the CCD clocking signals from the Electronics Box 15 to the Camera Body 20 (Figure 3). When this system was developed, the Astronauts felt that it was important in some cases to make the Camera Body 20 detachable, hooked up with a six foot cable 64. For these lengths it is important to use a differential line driving and receiving circuit. The RS-422 Differential Line Receiver was chosen to be the standard on this cable due to its high speed and long line driving capability.

The power supplies for this circuit are illustrated in the lower left hand corner of the schematic of Figure 14A and generally comprise Zener diodes, 211, 212, integrated

circuits ("IC's") 221, 222, 223, 224, 225, 226, and 227 and supporting circuitry. The CCD 210 (Figure 14B) requires a large number of different voltage levels for its operation. To decrease the number of wires in the power cable 64 between the Electronics Box 15 and the Camera Body 20 only +5VD, DGND, +12V and -12V voltage lines are connected as input signals to this circuit. Also, by using local regulated power supplies, the induced noise is much less than it would be if all of the necessary voltage levels were run by voltage lines all the way from the Power Supply 85 (Figure 2) located in the Electronics Box 15. The power supplies 205 in the CCD PCB 200 preferably are also "programmable" so that the CCD 210 can be optimized for specific mission related parameters. Some of the parameters which may be changed preflight by adjusting these levels are the amount of antiblooming, the full well capacity, radiation hardness, spurious charge reduction and output amplifier gain.

The Output Drain referred to in the drawing as "OD" of the CCD 210 has a high voltage requirement. A DC / DC converter 221 preferably is included to convert the incoming +12V up to +24V at a full load efficiency of 78%. The +24V then is regulated by voltage regulator 222 down to +20V. The resistors on the outputs of each of the regulators are in place to meet minimum current requirements. Zener diodes 212 and 211 are used for the +1.22V and +8.4V voltage supplies, respectively. The current requirements are very low for these two supply voltages so the use of Zener diodes 211, 212 is satisfactory. The LM317LZ (222, 223, and 224) and LM337LZ (225, 226, and

227) voltage regulators that are used for the other potentials in this design have a minimum current draw which is much higher than the current required by 212 and 211.

Referring still to Figures 14A and 14B, the level shifting circuitry constructed in accordance with the preferred embodiment comprises transistors 232 through 259. The Level Shifting circuits 90 take TTL (Transistor Logic) levels in, with less than 0.8V equating to a low level and greater than 2.0V equating to a high level, and provide a voltage output through the two output transistors such as 233 and 234. For example, the level shifting circuit made up of 232, 233, 234 and 235 takes in either a 0V or +5V input signal from the AOUT output of Line Receiver 202 (pin 3). This signal is input at the emitter of transistor 232 and is converted to a +3V output at the emitter of transistor 233 when 0V is at the input (the emitter of 232). Conversely, a -9V output is obtained at the emitter of transistor 233 when +5V is at the input (the emitter of 232). The parts used for this level shifting design are critical. The turn on and the turn off times must be very short. In this design, Part No. 2N4260, made by Motorola, is used due to its 1ns turn on and turn off times. While this design does not necessarily require this fast speed, the flexibility preferably is available in situations where the driving electronics must be set up for a faster rate. Slower turn on and turn off transistors have been tested resulting in unusable circuit characteristics. One skilled in the art will note that this level shifting design does not employ negative feedback. Leaving out negative feedback insures that large current transitions will not occur during a voltage level hold period.

The CCD 210 preferably drives a preamplifier output circuit 35 (Figure 14B) comprising operational amplifier 265, voltage regulator circuit 267, and transistor 269 to buffer and boost the CCD's output. The CCD 210 has internal to it a source follower field effect transistor ("FET") amplifier. The Output Drain ("OD") shown on pin 5 of the CCD 210 in the preferred embodiment and Output Source ("OS"), shown on pin 4, are the connections of this internal amplifier to the outside world. Resistor 271 comprises the load resistor for the CCD's internal FET. The value of resistor 271 can be changed by one skilled in the art to optimize the characteristics of the individual CCD 210. It should also be noted that noise and gain parameters are affected by this resistor's value.

The output signal from the CCD 210 is AC coupled to an operational amplifier 265 by capacitor 272. Resistors 273 and 274 set the output of amplifier 265 at a DC midpoint for proper operation from a +9V voltage supply, comprised of voltage regulator 267. Operational amplifier 265 is configured as a programmable supply current, current feedback amplifier with a gain of 10, bandwidth of 35 Mhz, 70mV integrated noise and a current draw of only 1.2 ma. Voltage regulator 267 ensures that its power supply is clean and that it is not supplying voltage beyond the amplifier's maximum supply voltages. Transistor 269 is an emitter follower used to drive the cable between the CCD PCB 200 and the Analog PCB 300 (Figure 13). The emitter follower configuration provides a low impedance output with a high current potential. Resistor 276 and capacitor 277 are the programming resistor and capacitor for the amplifier 265.

The CCD 210 used in the preferred embodiment of Figures 14A and 14B is the Ford FA1024L. As mentioned above, this camera can support a 1024 x 1024 monochrome, a 2048 x 2048 monochrome and a 2048 x 2048 color CCD. The Ford CCD is a 3 phase, two output, MPP (Multi-Pinned Phase) Implant, 1 megapixel per second readout device. It preferably is run in an antiblooming mode to suppress excess charge which would normally cause blooming up and down the CCD columns. When one starts an investigation on how to build a high performance electronic camera system based on a CCD, it is found that the way the CCD is run or clocked out determines the foundations for the performance of the camera system. Clocking techniques determine many of the parameters of the CCD's performance.

In the preferred design, the CCD 210 is clocked out only one of the outputs (pin 4). The CCD 210 typically is made so that half of the device can be read out the top and half out the bottom or all of the device out the top or bottom. The advantage in running the device only out one side is that there is no need to coordinate the output signals from the two halves with each other. In other words, separate outputs can have separate characteristics giving half of the image a different offset or gain or noise character. When the device is run out only one output, there is no noticeable split between the two sections when an image is viewed. With carefully designed circuitry, multiple output devices may be run in a multi-output mode. This would, of course, require two support circuits for each output. Because the readout rate is near 1 megapixel per second and the CCD array

contains 1024 x 1024 pixels, the device can be read out in about 1 second. If a faster output is required, it may be necessary to use both CCD outputs.

As mentioned above, the preferred design clocks the CCD 210 in an antiblooming mode. This mode of operation has been generally known for some time but has been recently brought into use, motivated by this ESC project. The antiblooming technique used in the preferred embodiment is referred to as Clocking Recombination Antiblooming ("CRAB") and it has several advantages. The CRAB technique does not decrease the sensitivity of the CCD, it does not reduce the fill factor of the CCD (how much area is active on the face of the sensor), but it can suppress a very large amount of excess charge. There does appear to be a shift in the MTF (Modulation Transfer Function) when the CCD is being used in the antiblooming mode. The preferred CCD is a three phase device with a Boron, multi-pinned phase ("MPP"), Barrier Phase implant under phase 3. (MPP will be discussed later). Phase 3 is biased to -9V during light integration. Phase 1 and 2 are clocked in such a way as to "slosh" the collected charge back and forth during integration. These phases are clocked from +6V to -9V. This technique brings the excess charge into a region that permits discharge through the channel stops, thus maintaining the maximum full well to a defined limit. By discharging the excessive charge with this technique, the camera can suppress spots of excessive light level without degrading the exposure of the rest of the image. This technique is extremely important for the successful operation of this system.

The ESC can be operated in two preflight set modes, the CRAB antiblooming mode (preferred) as described above or the MPP mode. The MPP mode gives better dark current characteristics than the CRAB antiblooming mode but it cannot suppress excess charge. It also has a smaller full well capacity. The full well of the CRAB antiblooming mode is on the order of 150,000 electrons, the MPP mode is around 80,000. The pixel to pixel nonuniformity tends to be better in the CRAB antiblooming mode, around 1%. These two modes are easily changed by reprogramming one programmable logic device in the camera. All other parameters stay the same.

Because the ESC is designed to be a low power device and to work with a shutter, a certain sequence is followed for each image-taking event. First, the CCD 210 is cleared of charge by turning on the serial gates at the top of the device, turning on the reset gate and then running the array gates enough times to clear out the excess stored charge which builds in the CCD when it is idle. Second, the shutter is opened and the CCD's pixels are filled with electrons in response to the image focused on the CCD 210 by the camera lens. Third, the shutter is closed and the CCD 210 is read out one pixel at a time to the output circuit. This scheme allows the CCD 210 to run only from a time immediately before taking a picture until a time immediately following the picture taking. Because the CCD 210 is not run continuously, power is conserved. This technique also gives images on demand so that the user does not have to wait for the camera to take a picture. One dumping cycle of the CCD takes approximately 32 milliseconds. *See* Figure 31. This design currently dumps the CCD three times which means the time from when the

operator presses the shutter release button on the camera until the shutter fires is approximately 96 milliseconds.

According to the preferred embodiment, a large CCD, 15mm X 15mm, is used so that more of the 35mm format is used. This facilitates the use of the viewfinder. The viewfinder 18 (Figure 3) has been customized in the Camera Body 20 to show only the area viewed by the CCD 210. In addition, the CCD 210 has been modified to eliminate the protective glass covering with which it is normally obtained. It was found that the glass covering commonly used on CCD's produced a large amount of noise due to reflection off of the interior components of the camera. Removing the glass greatly reduces these reflections and the ensuing noise. An alternative solution is to cover the glass with an antireflective coating.

According to the preferred embodiment, a relatively large pixel size is used. As a result of using a larger pixel size, 15 microns x 15 microns, the optics are not under stress. Consequently, the ESC is not limited by the optics. Smaller pixel cameras have difficulty achieving a good modulation transfer function ("MTF") at their maximum resolution, due to the optical limits of their system. As shown in Figure 6, the Quantum Efficiency of this CCD is at a maximum of 45% at 6500 Angstroms. This can be shown to be superior to film or the human eye. The dark current of this CCD can be shown to be on the order of 25 Pa /cm^2 when run in the MPP mode. This is about two orders of magnitude better than other CCDs. The linearity of the Ford CCD has been shown to be within ±1%. Pixel to pixel nonuniformity has been tested to be within 1%.

B. ANALOG PCB

Referring now to Figures 13A, 13B, 16A and 16B, the Analog PCB 300 preferably comprises two circuits, the Analog Circuit 350 and the Camera Interface Circuit 325. These circuits are not related except for the fact that they both preferably are located inside the Camera Body 20.

1. Analog Circuit 350

The Analog Circuit 350 preferably includes Correlated Double Sampler circuitry 40, Sample and Hold circuitry 45, an Analog-to-Digital Converter 60, and a Line Driver 61. The function of the Analog Circuit 350, in overview, is to receive the output from the CCD 210 by way of the CCD preamp 35, (comprising amplifier 265 in Figure 14), process the signal, digitize it and then send it to the Electronics Box for further processing and storage.

Referring now to Figures 16A and 16B, the output signal from the CCD PCB 200 is designated as VIN. It should be noted that the electrical conductor between the CCD PCB 200 and the Analog PCB 300 preferably is less than 30mm. The gain of this incoming signal VIN is controlled by variable resistor 301. The signal then is AC coupled to the two buffers, transistors 302 and 303. The circuit that comprises integrated circuit 305 and operational amplifier 306 is a correlated double sampling ("CDS") circuit 40. The CDS circuit 40 performs a subtraction of the reset level of the CCD output from the live pixel output. If this procedure is performed with the right timing, the correlated noise can effectively be subtracted out. The noncorrelated noise still remains. This

operation is implemented by delaying the reset level by 400 nS using the delay circuit, 305. This signal is fed to the inverting input of the opamp 306, which preferably is designed as a difference amplifier. The live pixel is fed to the noninverting input of amplifier 306. At the end of the live pixel time, difference amplifier 306 has the difference of these two signals on its output line 306. This output is sampled and held by integrated circuit 310, which comprises the Sample and Hold Circuit 45. Transistors 302, 303, and 304 are used as buffers and impedance matching circuits. The delay circuit 305 acts as a transmission line with an input and output impedance of 100 Ohms. It is important to match the impedance of the delay circuit 305 to prevent reflection and attenuation of the signal along the delay path to the difference amplifier 306.

The combined gains of the CCD Preamp 35 (Figure 14), the Correlated Double Sampler ("CDS") circuit 40 (Figures 16A-B) and the Sample and Hold circuit 310 (Figure 16) boost the CCD image signal up to 10Vpp. Black equates to 0V and Peak White is +10V. This is the signal required for the Analog to Digital Converter 60, shown as integrated circuit 360 in Figure 16B.

The ESC Electronic Still Camera is unique in that it uses 8 bits out of a 12 bit A/D converter 360 to insure that the digitizing is accurate to 8 bits. Most devices use 8 bit converters which are accurate only to about 5 bits. This is one reason why this Camera has achieved superior performance levels. Integrated circuits 351 and 356 are RS-422 line drivers to differentially drive the data lines between the Camera Body 20 and the Electronics Box 15.

The integrated circuits ("Ics") used in the preferred Analog Circuit are heavily bypassed. With analog and digital signals on the same printed circuit board, noise problems are numerous. The circuit constructed in accordance with the preferred embodiment employs a separate analog and digital ground. The Analog PCB 300 is designed with as much space as possible covered by the analog ground plane. Ferrite beads 321 are used along with decoupling resistors on difference amplifier 306. The Ferrite Beads 321 guard against oscillations on the power supply lines, and the resistors decrease the voltage level of any power supply line noise at the difference amplifier 306. The capacitors used in conjunction with the decoupling resistors give the operational amplifier 306 its own charge storage source for fast transients by remaining isolated from the rest of the circuit.

Referring still to Figures 16A and B, variable resistors 301, 307, 308, 309 and 311 preferably are the adjustments for the analog circuit. As mentioned above, variable resistor 301 adjusts the incoming gain. Variable resistor 307 is used to match the impedance of delay circuit 305. This adjustment is critical to maintain the integrity of the signal in the delay line. Variable resistor 308 establishes the DC offset needed for Sample and Hold Circuit 310. Variable resistors 309 and 311 adjust the zero level and gain of the Analog to Digital Converter 360.

As noted above, some circuits which have been designed to perform a similar function as the CDS Circuit 40 use multiple analog switch integrated circuits. The large transients caused by analog switches combined with the fact that the turn on to turn off

ratio is poor, makes these types of designs exhibit a lower performance. The less switching the better for a circuit of this type.

Difference amplifier 306 also is used as a filter to limit the noise bandwidth of the analog chain. An optimum bandwidth has been chosen to limit as much noise as possible but still insure that the pixel value could be reached before the sample and hold circuit took its sample. This is accomplished by the selection of capacitors 313, 317 and 319.

The DC voltages needed for the operation of the Analog Circuit are obtained on the Analog PCB 300 by the DC / DC Converters, 326, 327, 328 and 329. As with the CCD PCB 200, using local power supplies gives better noise performance and cuts down on the number of wires running from the Electronics Box 15.

2. Interface Circuit 325

Referring now to Figures 15, 17, 31 and 32, there are three triggering signals, N1, N2 and N3 which pass between the Camera Body 20 and the Electronic Box 15. The schematic of the Camera Interface Circuit 325 shown in Figure 17 illustrates the circuit which performs those functions.

Referring now to Figure 17, the Camera Interface Circuit 325 constructed in accordance with the preferred embodiment includes integrated circuits 365 and 366 as RS-422 Line Drivers and Receivers respectively to communicate to the Electronics Box 15 (Figure 3). When the shutter release button (not shown) on the Camera Body 20 is pressed, the signal RB2 goes low. The RB2 signal is supplied as an input signal to invertor 371, which inverts the low signal RB2 on its input to a high signal, N1 on its

output. The signal N1 is transmitted to the Electronics Box 15 via Line Driver 366. After a short delay during which the CCD 210 and other circuits are readied for picture taking, a pulse N2 is received in the Line Receiver 365 from the Timing Generator 75. When N2 goes high, transistor 373 turns on, pulling RT to ground, which fires the shutter. The signal XSYNC then is received from the Camera to represent that the shutter has closed. From the XSYNC signal, a signal N3 is generated, which is used by the Timing Generator 75 in the Electronics Box 15 to know when to proceed with the picture taking cycle. The line labelled NGND in this design is Digital Ground. Diodes 381, 382, resistor 376 and capacitor 374 are used for noise immunity.

C. MEMORY PCB 400

Referring now to Figures 13A and 13B and 18A-C, the preferred embodiment of the Buffer Memory Circuit 65 will be discussed. The Buffer Memory circuit 65 supports both 1 Megabyte and 4 Megabyte static random access memories ("SRAM's") for running the 1K x 1K or 2K x 2K CCDs respectively. SRAMs are used in the preferred embodiment to cut down on noise and power consumption which would be a problem if dynamic random access memories ("DRAM's") were used. The memory circuit is located on the Memory PCB 400 in the Electronics Box 15. The signals D0-, D0+, D1-, D1+, etc. are the incoming image data lines from the Analog-to-Digital converter 360 on RS-422 Line Driver 351 and 352 in Figure 16B. At the time that image data is valid and enough settling time has passed, the MEMWR signal is activated writing each pixel's value to a memory location. The signals INCC, INCADD, RESETC and CAMST are

used to increment and reset the counters 401 through 406 which produce the addresses for the memory bank 425, which comprises integrated circuits 412 through 419. The addresses are reset before image storage in the memory bank 425 and also before the memory bank 425 is read out and transferred to the Permanent Memory 80. The incrementing signals are used in the same way, one for image storage and one for read out. The data lines for read out are 00 through 07. The selection of 4 Megabyte or 1 Megabyte memory architecture is made by the jumpers JMPR1 through JMPR8.

D. DIGITAL PCBs

Referring now to Figures 13A-B, 19 and 23, the Digital processing circuitry preferably is contained on two separate printed circuit boards, referred to herein as Digit 1 PCB 500 and Digit 2 PCB 600. The Digit 1 PCB 500, shown in Figure 19, includes the Microcomputer Circuit 550, the Hard Disk Interface Circuit 525 and the I/O Port Circuit 575. The Digit 2 PCB 600, shown in Figure 23, preferably includes the SAM Digital Circuit (Timing Generator) 650, the Downlink Interface Circuit 625 and the L3 RS232 Interface Circuit 675.

1. DIGIT 1 PCB 500

a. Microcomputer Circuit 550

Referring now to Figures 19, 20A and 20B, the Microcomputer Circuit 550 generally comprises the Intel Wildcard 88 single board computer 555, a dynamic random access memory ("DRAM") module 560, and a DRAM interface. The Wildcard computer 555 has on its connector a superset of the IBM XT bus. Physically, the Wildcard 555 is

2" x 4", runs at 10MHz and operates at about 1 watt. This Computer 555 is used to run the Camera's hard drive, communicate with the RS232 port, run the camera's downlink circuit, perform low power operations with the camera's power supply, interface to the camera's SRAM memory buffer for image data acquisition, run the LCD display, take commands from the camera's controls and interface to the date and time clock. The BIOS (Basic Input Output System) for this Computer 555 preferably is a NASA custom BIOS produced for this design. The Computer 555 operates as a standard XT but in an embedded capacity. The programs which the Camera uses to execute its operations are preferably loaded from the permanent memory hard drive 80 after the boot-up period is complete. Initial camera boot up currently takes 20 seconds. The camera's programs are a combination of 'C' and Assembler. An example of a program for this Microcomputer design is attached in the Appendix.

Referring now to Figures 20A and 20B, a keyboard connector 548 is used to hook up an XT style keyboard (not shown) for system testing and development. Connector 549 obtains the signals needed to implement a DMA (Direct Memory Access) circuit for high speed downlink systems such as the Orbiter's KU channel 3, with 48 Mbits per second link. The rest of the Microcomputer circuit 550 in Figures 20A and 20B is used as DRAM and DRAM support. Integrated circuits 504, 503 and 502 are used for addressing the DRAM 560. Integrated Circuit 505 is a bidirectional data buffer which transmits the DRAM's output data onto the system bus 515. The Microcomputer circuit 550

communicates to the rest of the Camera through the output signals including D0-D7 and A0-A19, located on the right side of Figure 20B.

The data and time clock (not shown) is a No-Slot Clock. It preferably plugs into an EPROM socket such as the one for the Microcomputer BIOS or the Hard Disk BIOS but allows the EPROM to be replugged in on top of it, and thus no slot is used. This clock uses its own software which is initialized during camera boot up. Alternatively, when the L3 system is used, the clock input can be derived from the L3 electronics.

b. Hard Disk Interface Circuit 525

The Hard Disk Interface Circuit 525 is part of the DIGIT 1 PCB of Figure 19 and is shown in more detail in Figures 21A-B. Referring now to Figures 21A-B, the left side of the circuit schematic (Figure 21A) shows the IBM bus (including D0-D7 and A0-A19) through which this circuit communicates to the Microcomputer Circuit 550. The heart of this circuit is the EPROM 530 (Figure 21B) which contains a Disk Drive BIOS produced by Western Digital. The XT Microcomputer BIOS does not make provisions to run a hard drive so this capability has to be installed in this location. The address location for the hard drive is C800:0000. This address is decoded using a combination of the address lines of EPROM 530 and the combinational logic 533, 534, 532, and 531. The programs contained in the hard drive BIOS revector the disk interrupts such as INT 13H and INT 40H to locations in this BIOS. According to the preferred embodiment, these routines control the hard drive and determine its operating character. The hard disk BIOS is actually executed during the Microcomputer's boot up sequence. It is here that

these vectors are rerouted. Integrated circuit 537 serves as a data buffer to the IBM data bus.

Connector 542 feeds power to the hard disk, while connector 520 is the signal connector for the hard drive. The hard drive used in this camera preferably is made by Prairie Tek. The camera supports both the 20 Megabyte Model 220 and the 42 Megabyte Model 240. Both are removable and act as a substitute for a conventional film cartridge. The specifications for these drives can be found in the literature supplied by Prairie Tek. The features of the Prairie Tek which are particularly advantageous includes a power down mode, auto parking heads, 100G shock capacity, 1.625 MBytes per second write speed, small size and light weight. The LED, 522 lights when the drive is active.

c. I/O Port Circuit 575

The I/O Port Circuit 575 is included in the Digit 1 PCB 500 of Figure 19, and is shown in detail in Figure 22. The objective of the I/O Port Circuit 575 is to interface the Microcomputer circuit 550 to the various elements with which it needs to communicate. These elements include the Memory Buffer Circuit 400, the SAM (Stand Alone Microsequencer) 650, the Mode Select Switch 27 (*see* Figure 3), the power supply circuit 825, downlink circuit (High Speed Data Port) 130, LCD circuit 700, Standard Data Port 120 and the Permanent Memory Circuit 80.

The advantage of the I/O Port 575 of the preferred embodiment is that it is fast and it consumes practically no power when not operating, 8uA per part. The disadvantage is that it is not very versatile. Throughout this design, the SSI and MSI

parts are ACT (Advance CMOS Technology). These were chosen due to their short propagation delays and their low power as pointed out above. Also, they are compatible with standard TTL parts.

Referring still to Figure 22, there is shown on the left side of the circuit the signals received from the IBM buss. Addresses are decoded and decisions are made as to whether an operation is a read or a write by the rest of the logic. The address decoding makes sure that the right data is sent to the right peripheral. Integrated circuits 585 and 586 are multiplexers used to input either the camera's data or to control signals. These signals are then put on the camera's internal data bus labeled B0 through B7. This bus also is used for the LCD and Downlink data. All other signals at the right hand side of the drawing are outputs. PWRUP is used to put the power supply in a low power mode. INCC and RESETC were previously discussed. CAMST is the signal which is used to turn logic control over to the SAM circuit 650 and initialize a picture taking sequence. LCD Latch latches the LCD data when its address has been decoded. DL Latch latches downlink data when its address has been decoded.

2. *DIGIT 2 PCB 600*

a. SAM Digital Circuit 650

Referring now to Figures 23 and 24, the Stand Alone Microsequencer ("SAM") Digital Circuit 650 (comprising the Timing Generator 75), constructed in accordance with the preferred embodiment, generally comprises the SAM integrated circuit 655 and the Line Drivers and Receivers 656-659.

Referring now to Figure 24, the main component of the SAM Circuit is the Stand Alone Microsequencer IC 655. This integrated circuit communicates with the Camera Body 20 by the RS-422 line drivers and receivers, 658, 657, 656 and 659. The N3 signal which goes off the drawing as an output module port corresponds to the N3 of Figures 17, 30 and 31. The SAM IC 655 is an Erasable Programmable Logic Device ("EPLD"), and it preferably runs a program which is developed and loaded using the Altera Development System. This program contains the timing for clocking the CCD 210. When the camera is changed from the 1K x 1K to the 2K x 2K configuration, the program in the SAM IC 655 preferably is changed as well. The clock for the SAM operation comprises integrated circuit 651 which runs at 6.67MHz. This makes the primary period of the CCD 210 timing 150nS. The power up reset is produced by inverters 656, 657. The reset timing of the SAM 655 is critical to ensure that the SAM powers up in the right state. Integrated circuit 648, 649 comprise J-K flip flops that are is used to make the CAMST and N3 signal synchronous with the SAM's clock. This is necessary to ensure that the SAM 655 does not go off into an undefined state. The majority of the information on what is going on in this circuit is found in the SAM program, which can be found in the Appendix.

b. Downlink Interface Circuit (High Speed Data Port) 625

Referring now to Figure 25, the Downlink Interface Circuit 625 takes data in from the I/O Port 575 of the DIGIT 1 PCB 500 through the bus lines B0 through B7. The DL Latch input signal indicates when the downlink data is good and can be latched into the

shift registers 631 and 632. In order to keep the system synchronized, the clock input signal, CLK, which is used for downlinking, is the Microcomputer's system clock. The JK flip flop 633 preferably is used to reclock the data as it comes out of the shift register 632. For each byte of data transmitted there also is a signature byte produced by shift register 632 which precedes the data. This is provided, in accordance with the preferred embodiment, to meet some of the Orbiter's downlink criteria. When the DL Latch is high, the data is loaded from the data lines. When DL Latch returns low, the data shifts through the shift registers 631, 632, to the JK flip flop 633. The JK flip flop 633 drives the 50 Ohm line driver circuits 621, 622, that preferably are comprised of discrete components. The two driver circuits 621, 622 connect to the connector 626, which preferably connects to the Orbiter. The 50 Ohm line driving circuits 621, 622 take a TTL level signal in and output a near 0V to near 6V signal. In the preferred embodiment, these circuits 621, 622 drive an RG400 cable hooked between the ESC and the Orbiter (or an alternative transmitting station). Unlike most other coaxial drivers, driving circuits 621, 622 draw very little current when idle.

c. L3 RS232 Interface Circuit (Standard Data Port) 675

Referring now to Figure 26, the RS232 Interface Circuit 675 is shown in accordance with the preferred embodiment. The Interface Circuit 675 is based on an integrated circuit 670 comprising a UART (Universal Asynchronous Receiver /

Transmitter) that is often used in IBM compatible designs for serial communications. The UART 670 runs at a standard rate of 1.8 Mhz and has a programmable baud rate, as well as several other programmable parameters. These parameters are set automatically by the serial communications driver built into the BIOS and the DOS operating system. The connector port 680 can be used for any user data and, according to the preferred embodiment, is currently being planned to take in the L3 (Latitude Longitude Locator) data. The communications protocol is Kermit.

The address decoding for this circuit is accomplished in the I/O Port Circuit 575 on the DIGIT 1 PCB 500 (Figures 19 and 22). The E, A4, A0, A1, A2 input module ports come from the I/O Port Circuit 575 for this purpose. The RESET DRV is the standard IBM reset for all peripherals. The serial communications is set up for COM1 using IRQ4 (Interrupt Request 4). This is generated by the UART 670 and integrated circuit 685, according to another IBM convention. The RS232 Line Drivers and Receivers 672 and 671 are standard parts commonly used for this application. Line Driver 672 runs off of +12V and -12V supply, resulting in a +9V and -9V signal for a TTL level input. Line Receiver 671 receives RS232 level signals and converts them to TTL level. The resistor 677 allows communications even when input line DSR is not used. For this design, conventional software handshaking preferably is used. The DTR and DSR lines could be implemented for user data input protocol by changing the software in accordance with conventional techniques.

D. LCD PCB 700

The LCD Circuit 750 is shown in Figure 27 and forms part of the LCD PCB 700 shown in Figure 13. The LCD 725 used in the preferred embodiment is a 3.5 digit display unit. The LCD interfaces to the I/O Port circuit 575 of the DIGIT 1 PCB 500 through the LCD drivers 501 and 502. The data lines B0 through B7 are used for the interfacing. Integrated circuit 704 comprises the LCD clock, which drives the COM line of the LCD 725. The LCD 725 preferably includes a battery low indicator which is activated when the BATT LOW input line goes high. The BATT LOW line comes from the Power Supply 85 and indicates when the battery needs changing. The BATT LOW indicator flashes at a slow rate determined by the oscillator comprised of NAND gates 721, 722, 723, resistor 718 and capacitor 712.

E. POWER SUPPLY PCB 800

Referring now to Figure 28, the Power Supply PCB 800 contains two separate circuits, the Power Supply Circuit 825 and the Battery Low Circuit 875. As illustrated in Figure 28, these two circuits have a few external connections that determine their state. The Power Supply Circuit 825 preferably uses a NP-77H battery 811 as its power source input. This battery is a 2400mAH battery. The Power Supply Circuit 825 also interfaces to the Disk Microswitch, SW1 which shuts power down if the disk is being removed to guard against disk damage. The Battery Low Circuit 875 inputs the two reset switches SW2 and SW3 (29 in Figure 3) from the control panel, and outputs a reset signal UP RESET to the Microcomputer Circuit 550 to reset it if the operator has activated reset

switch SW2 or SW3 (25 in Figure 3). It also produces the signal BATT LOW to drive the LCD low battery input.

1. Power Supply Circuit 825

Referring now to Figure 29, the Power Supply Circuit 825 receives its energy source from the NP-77 Battery through the input module port labeled BATT. The power supply and the rest of the camera are turned on and off by the power on/off switch S1. The fuse F1 connects in series to provide circuit protection. Fuse F1 becomes critical if the camera is being run off the Orbiter's power instead of being battery operated. The Power Supply Circuit 825 can be operated off the Orbiter power (or for that matter, off of the power of an automobile or boat) by attaching a DC / DC converter to the battery terminals instead of using a portable battery. An LED 831 indicates that power has been applied. Diode 832 protects the camera from a reverse polarity source being hooked to the Power Supply Circuit 825. When power is applied, a DC / DC Converter 835 is activated if a disk drive is in place. The supply voltage EVER5V also is activated to run all of the ESC circuitry which requires a constant 5V supply. When the PWRUP signal is activated by the Microcomputer Circuit 550, +5V and +5VBAT are activated.

The MOSFET transistors 841, 842, and 843 that are used in this design have a very low voltage drop. They require a high voltage on the gates to operate effectively as a switch. As can be seen, all of them connect to the +12V supply. Transistor 841 is placed in the negative feedback loop of 847. In this configuration, opamp 847 adjusts the voltage at the gate of transistor 841 until the source of 841 matches the voltage on the

voltage divider 817. One advantage to this circuit is that in this configuration, transistor 841 has a very low drop voltage from drain to source. This is different than typical voltage regulators. It is important to use an opamp 847 such as the LM1458N to limit the bandwidth and avoid oscillations at the source of transistor 841. When the PWRUP signal is applied to the base of transistor 846, transistor 846 turns on, connecting the voltage source +12V to ground, and removing the voltage from the base of transistor 844, turning transistor 844 off. When transistor 844 turns off, MOSFET transistors 843 and 842 turn on. Because transistor 843 only turns on when the PWRUP signal is applied, battery power is conserved and temperature build-up is eliminated.

2. *Battery Low Circuit 875*

Referring now to Figures 3 and 30, the Battery Low Circuit 875 functions to detect when the battery has passed two thresholds. Sensing the first threshold it activates the BATT LOW signal, which starts flashing the BATT indicator on the LCD display 28 (Figure 3). Sensing the second threshold activates the UP RESET signal, which resets the Microcomputer Circuit 550 and holds it in the reset mode until the battery is changed. The manual reset switches 29 also can reset the Microcomputer Circuit 550 by way of the RESET SW as described above. These operations are accomplished by using the comparators 877, 879. The comparators 877, 879 check the polarity of the signals at the plus and minus inputs, compares those input signals and produces a differentiated output. The variable resistors 891, 893 are used to set the level where these operations occur.

While there has been shown what is considered to be the preferred embodiment of the present invention, it will be apparent to one skilled the art that many changes and modifications may be made herein without departing from the spirit of the present invention.

ABSTRACT

A handheld, programmable, digital camera is disclosed that supports a variety of sensors and has program control over the system components to provide versatility. The camera uses a high performance design which produces near film quality images from an electronic system. The optical system of the camera incorporates a conventional camera body that has been slightly modified, thus permitting the use of conventional camera accessories, such as telephoto lenses, wide-angle lenses, auto-focusing circuitry, auto-exposure circuitry, flash units, and the like. An image sensor, such as a charge couple device ("CCD") collects the photons that pass through the camera aperture when the shutter is opened, and produces an analog electrical signal indicative of the image. The analog image signal is read out of the CCD, and is processed by preamplifier circuitry, a correlated double sampler and a sample and hold circuit before it is converted to a digital signal. The analog-to-digital converter has an accuracy of eight bits to insure accuracy during the conversion. Two types of data ports are included for two different data transfer needs. One data port comprises a general purpose industrial standard port and the other a high speed / high performance application specific port. The system uses removable hard disks as its permanent storage media. The hard disk receives the digital image signal from the memory buffer and correlates the image signal with other sensed parameters, such as longitudinal or other information. When the storage capacity of the hard disk has been filled, the disk can be replaced with a new disk.

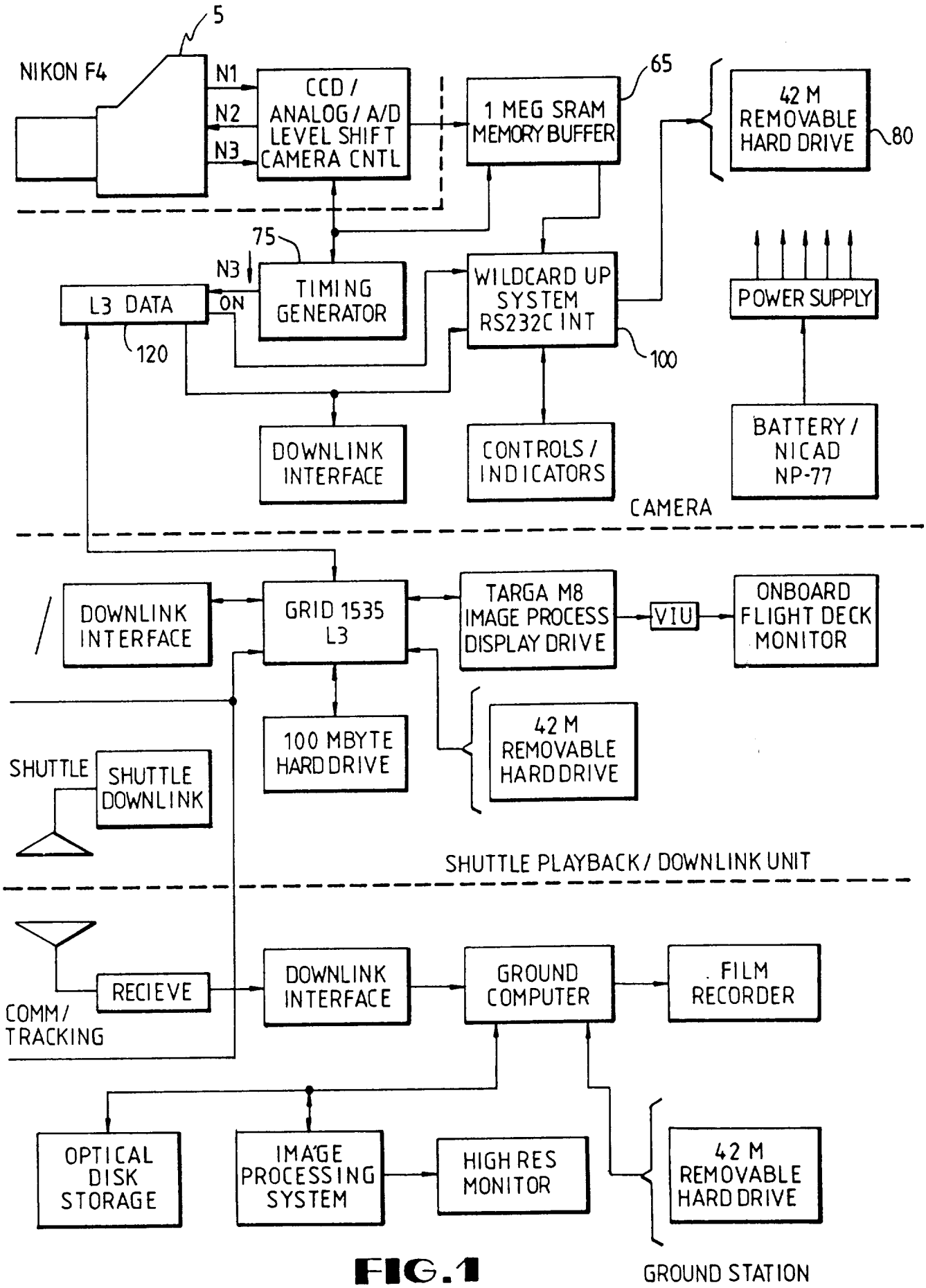

5
NIKON F4
N1
N2
N3
CCD / ANALOG / A/D LEVEL SHIFT CAMERA CNTL
1 MEG SRAM MEMORY BUFFER
65
42 M REMOVABLE HARD DRIVE
80
75
N3
ON
TIMING GENERATOR
L3 DATA
120
WILDCARD UP SYSTEM RS232C INT
100
POWER SUPPLY
DOWNLINK INTERFACE
CONTROLS / INDICATORS
BATTERY / NICAD NP-77
CAMERA
DOWNLINK INTERFACE
GRID 1535 L3
TARGA M8 IMAGE PROCESS DISPLAY DRIVE
VIU
ONBOARD FLIGHT DECK MONITOR
100 MBYTE HARD DRIVE
42 M REMOVABLE HARD DRIVE
SHUTTLE
SHUTTLE DOWNLINK
SHUTTLE PLAYBACK / DOWNLINK UNIT
RECIEVE
COMM / TRACKING
DOWNLINK INTERFACE
GROUND COMPUTER
FILM RECORDER
OPTICAL DISK STORAGE
IMAGE PROCESSING SYSTEM
HIGH RES MONITOR
42 M REMOVABLE HARD DRIVE
GROUND STATION

FIG. 1

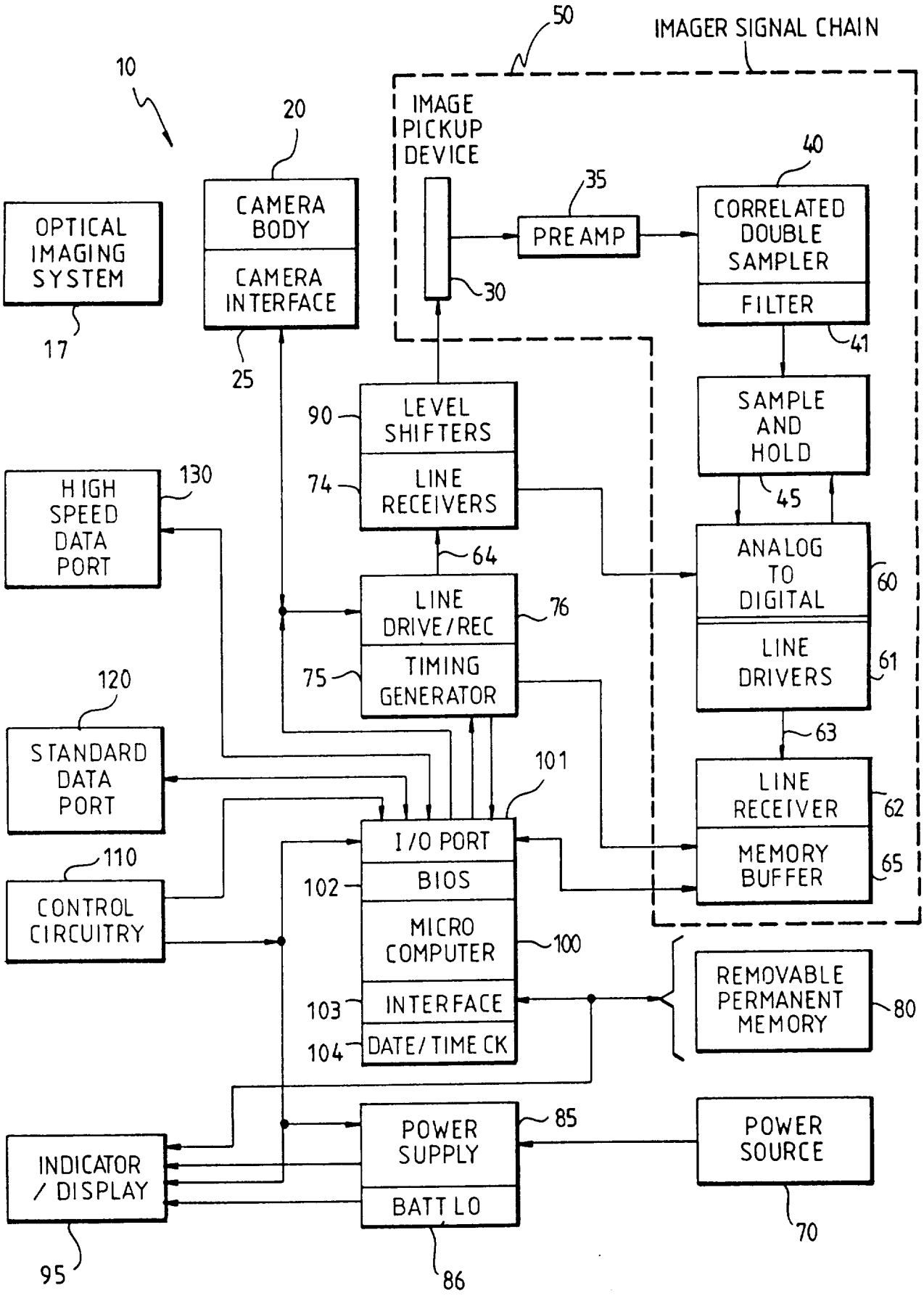

50
IMAGER SIGNAL CHAIN
10
20
IMAGE PICKUP DEVICE
40
35
OPTICAL IMAGING SYSTEM
CAMERA BODY
CAMERA INTERFACE
PREAMP
CORRELATED DOUBLE SAMPLER
FILTER
30
17
25
41
90
LEVEL SHIFTERS
SAMPLE AND HOLD
74
LINE RECEIVERS
130
HIGH SPEED DATA PORT
45
64
ANALOG TO DIGITAL
60
LINE DRIVE/REC
76
LINE DRIVERS
61
75
TIMING GENERATOR
120
63
STANDARD DATA PORT
101
LINE RECEIVER
62
I/O PORT
110
MEMORY BUFFER
65
CONTROL CIRCUITRY
102
BIOS
MICRO COMPUTER
100
REMOVABLE PERMANENT MEMORY
80
103
INTERFACE
104
DATE/TIME CK
85
POWER SUPPLY
POWER SOURCE
INDICATOR / DISPLAY
BATT LO
95
86
70

FIG.2

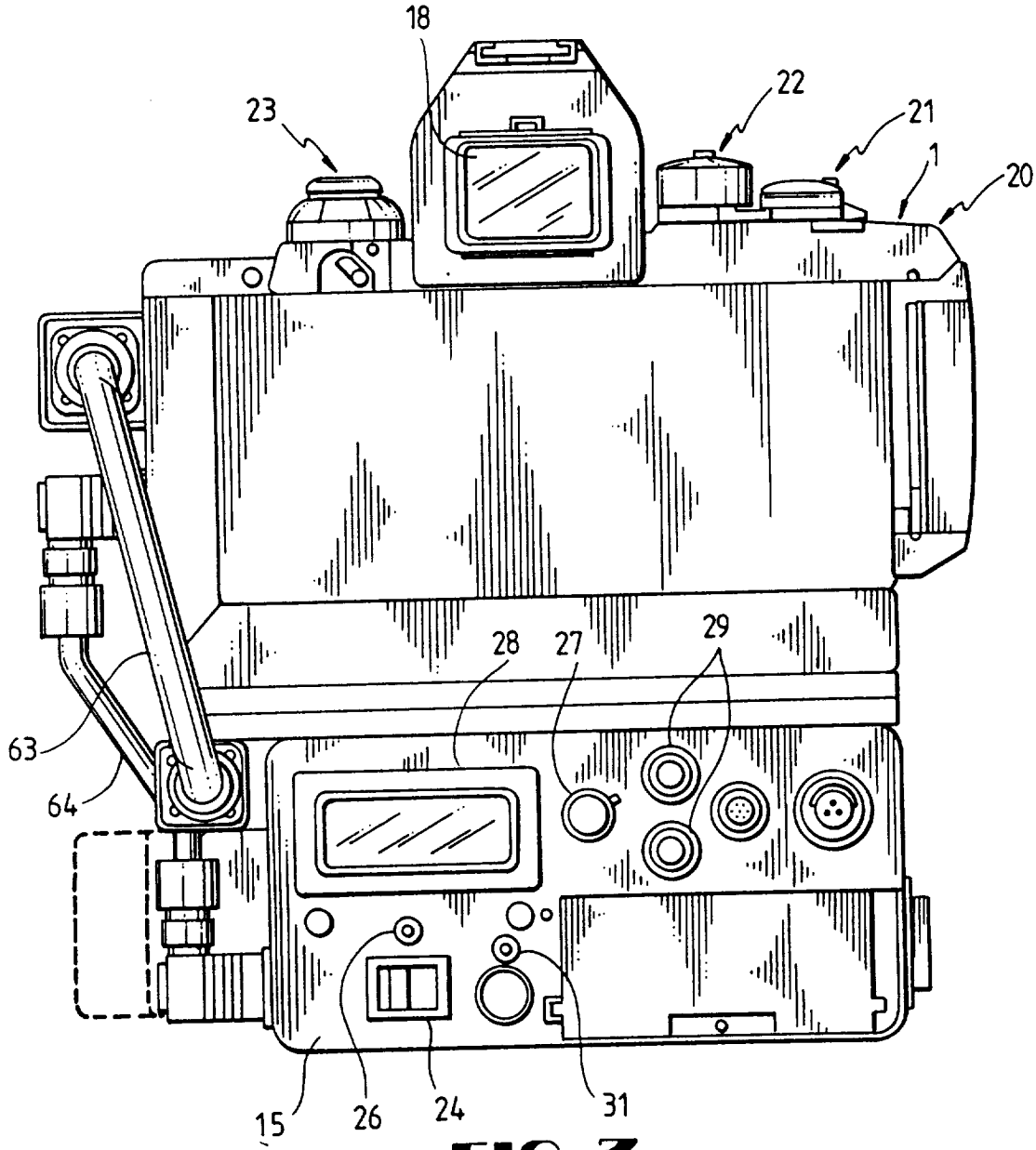


FIG.3

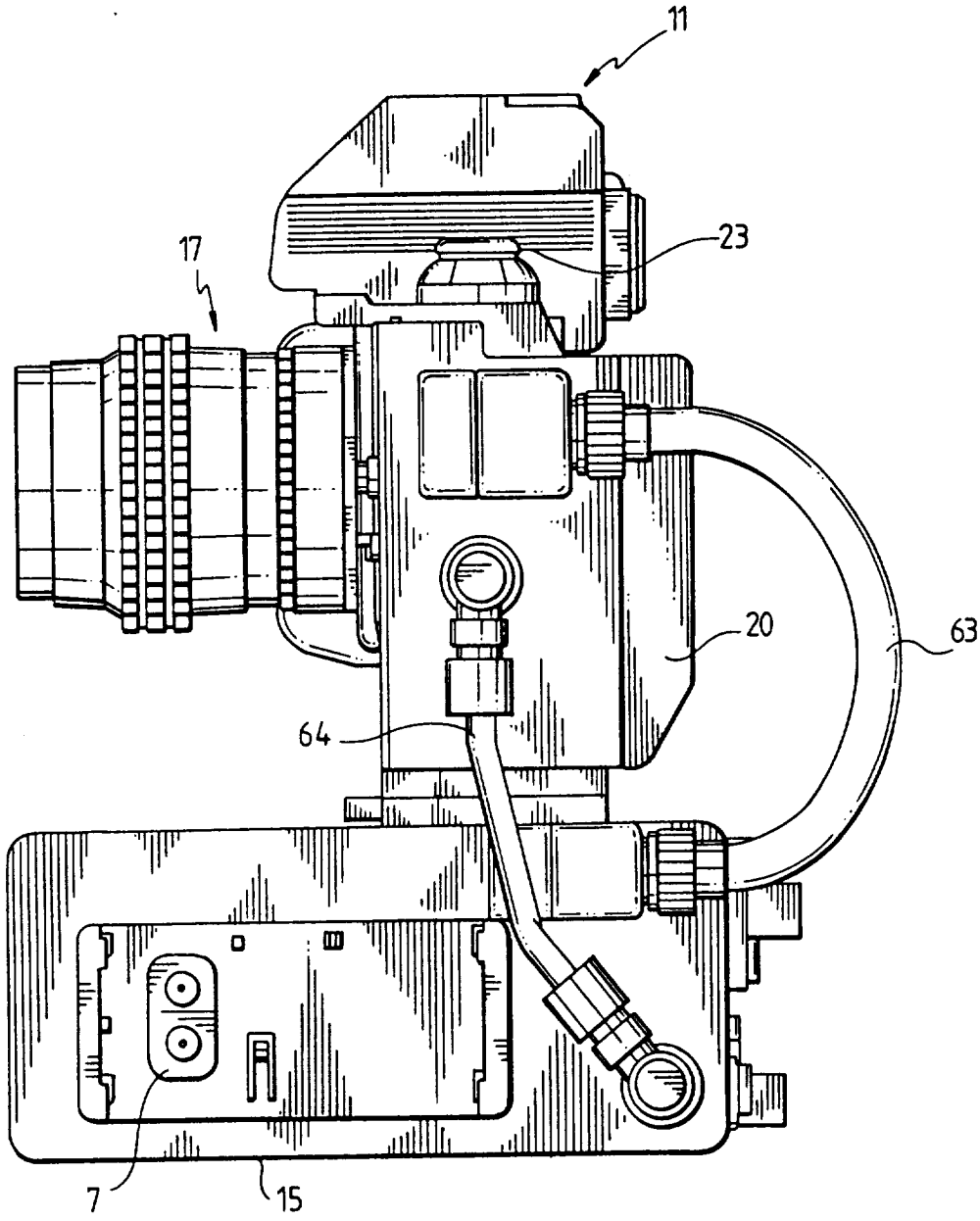


FIG. 4

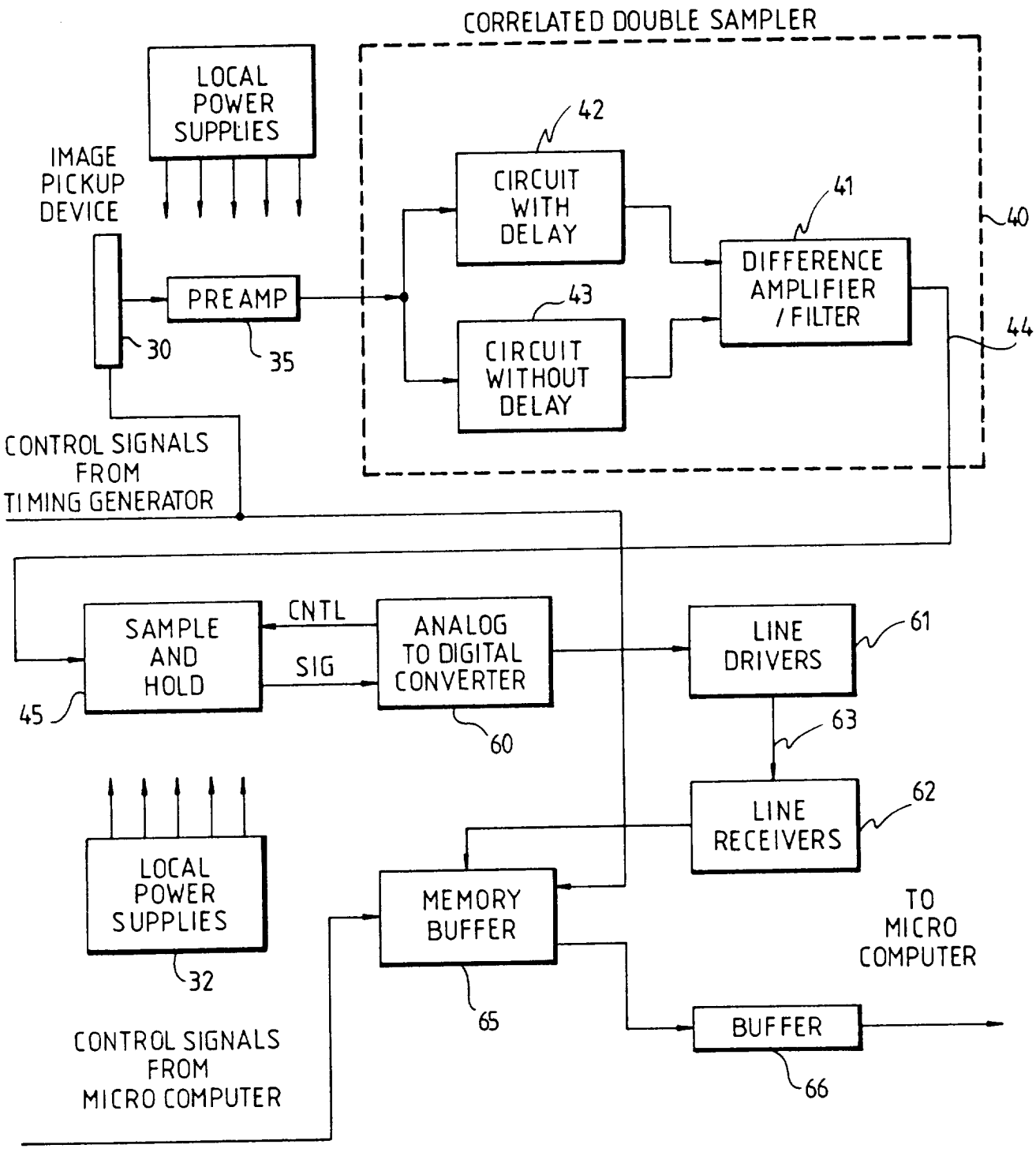

CORRELATED DOUBLE SAMPLER
LOCAL POWER SUPPLIES
IMAGE PICKUP DEVICE
PREAMP
30
35
42
CIRCUIT WITH DELAY
43
CIRCUIT WITHOUT DELAY
41
DIFFERENCE AMPLIFIER / FILTER
40
44
CONTROL SIGNALS FROM TIMING GENERATOR
SAMPLE AND HOLD
45
CNTL
SIG
ANALOG TO DIGITAL CONVERTER
60
LINE DRIVERS
61
63
LINE RECEIVERS
62
LOCAL POWER SUPPLIES
32
MEMORY BUFFER
65
TO MICRO COMPUTER
BUFFER
66
CONTROL SIGNALS FROM MICRO COMPUTER

FIG.5

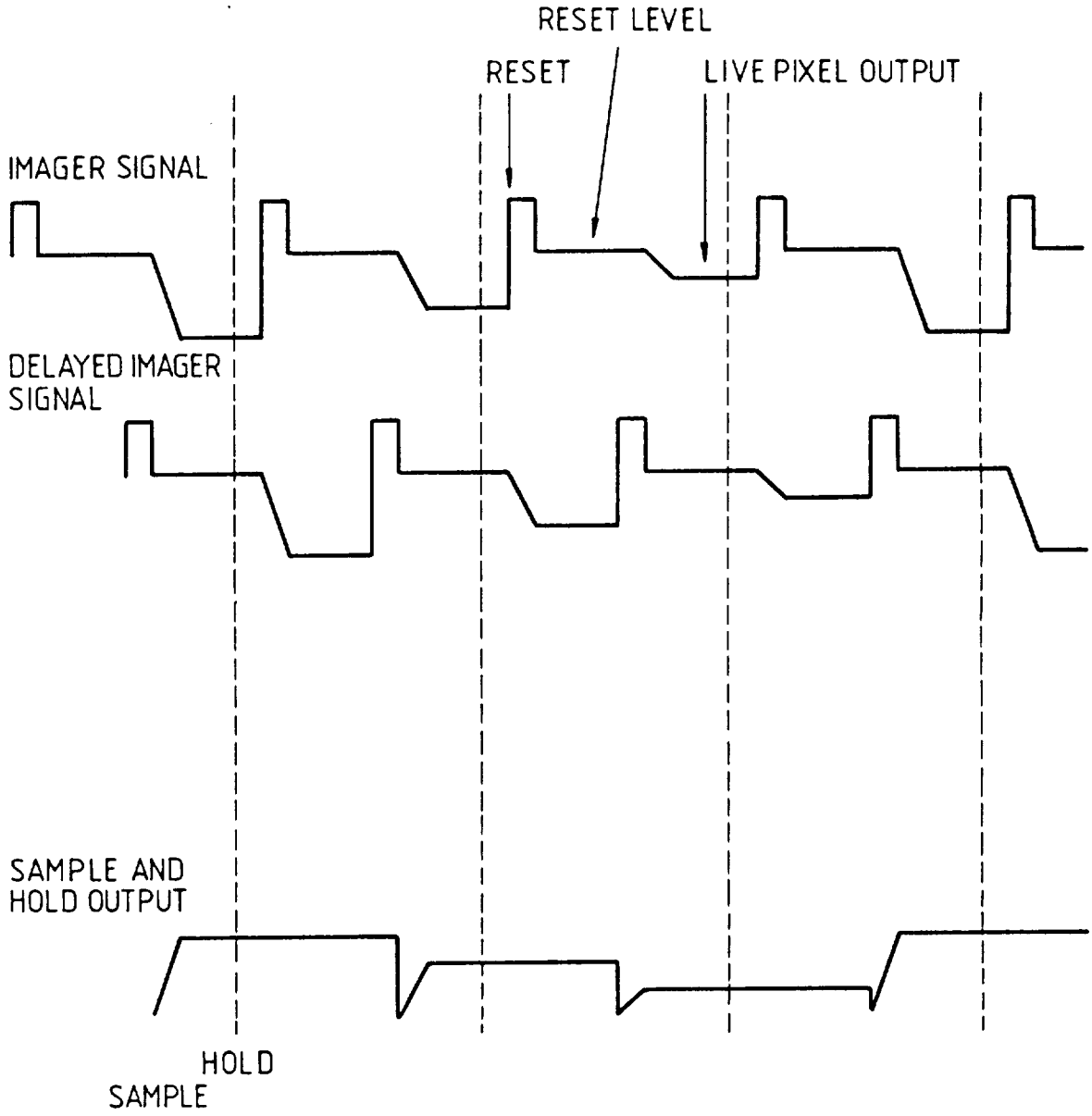
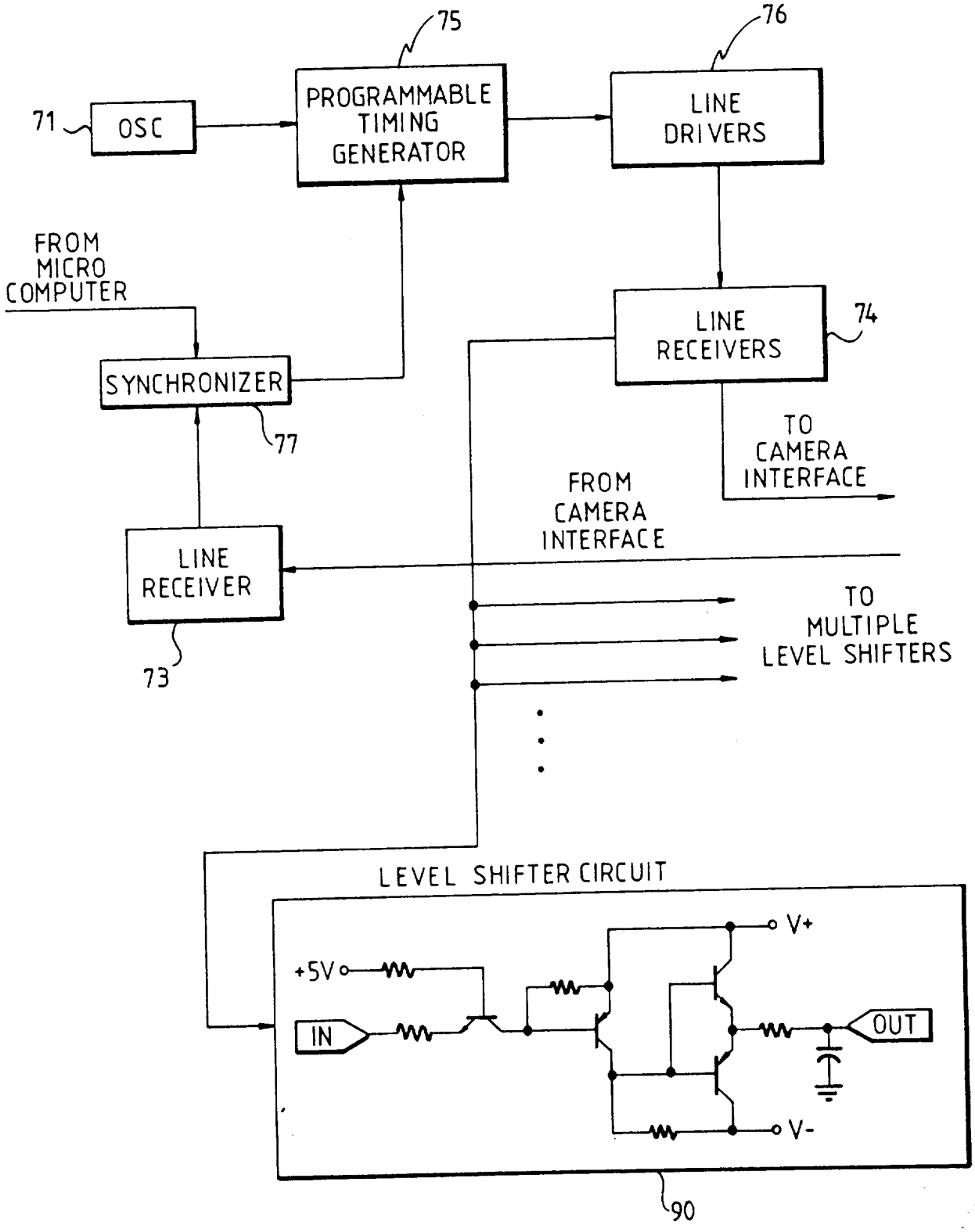
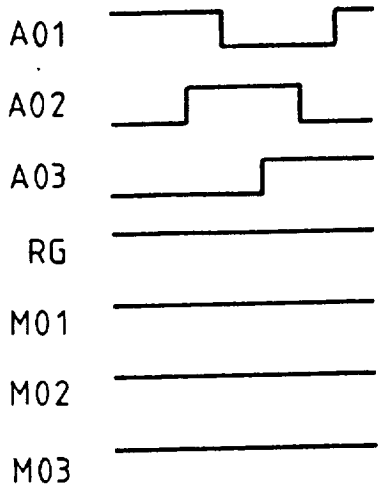


FIG.7

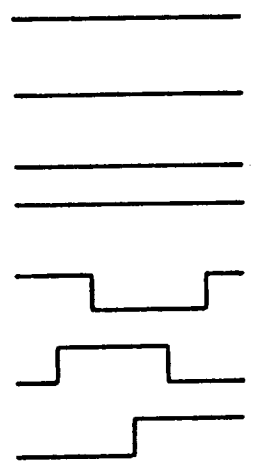
FIG.8


75
76
71
OSC
PROGRAMMABLE TIMING GENERATOR
LINE DRIVERS
FROM MICRO COMPUTER
LINE RECEIVERS
74
SYNCHRONIZER
77
TO CAMERA INTERFACE
FROM CAMERA INTERFACE
LINE RECEIVER
73
TO MULTIPLE LEVEL SHIFTERS
LEVEL SHIFTER CIRCUIT
V+
+5V
IN
OUT
V-
90



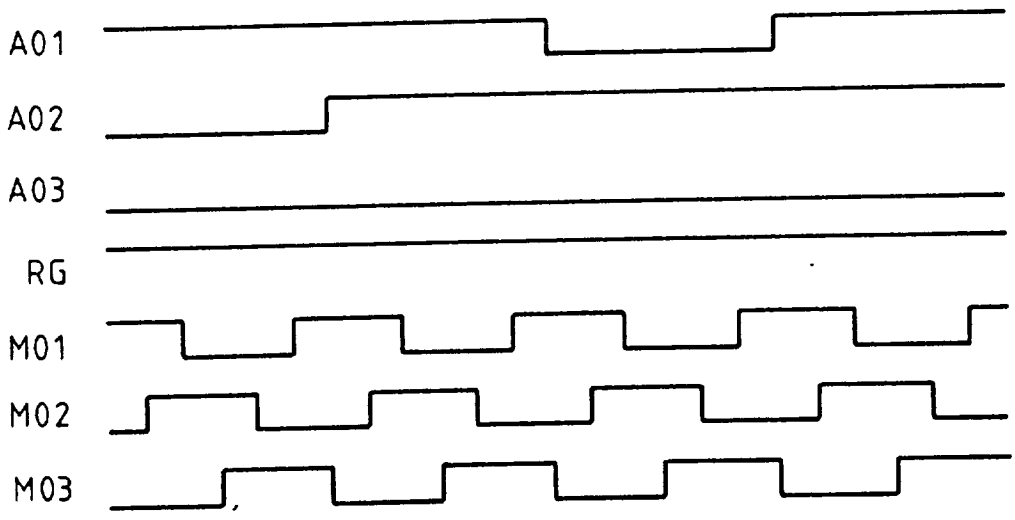
CHARGE DUMP 9.1

FIG.9A



MPP INTEGRATION 9.2

FIG.9B



TIMING WAVEFORMS

FIG.9C

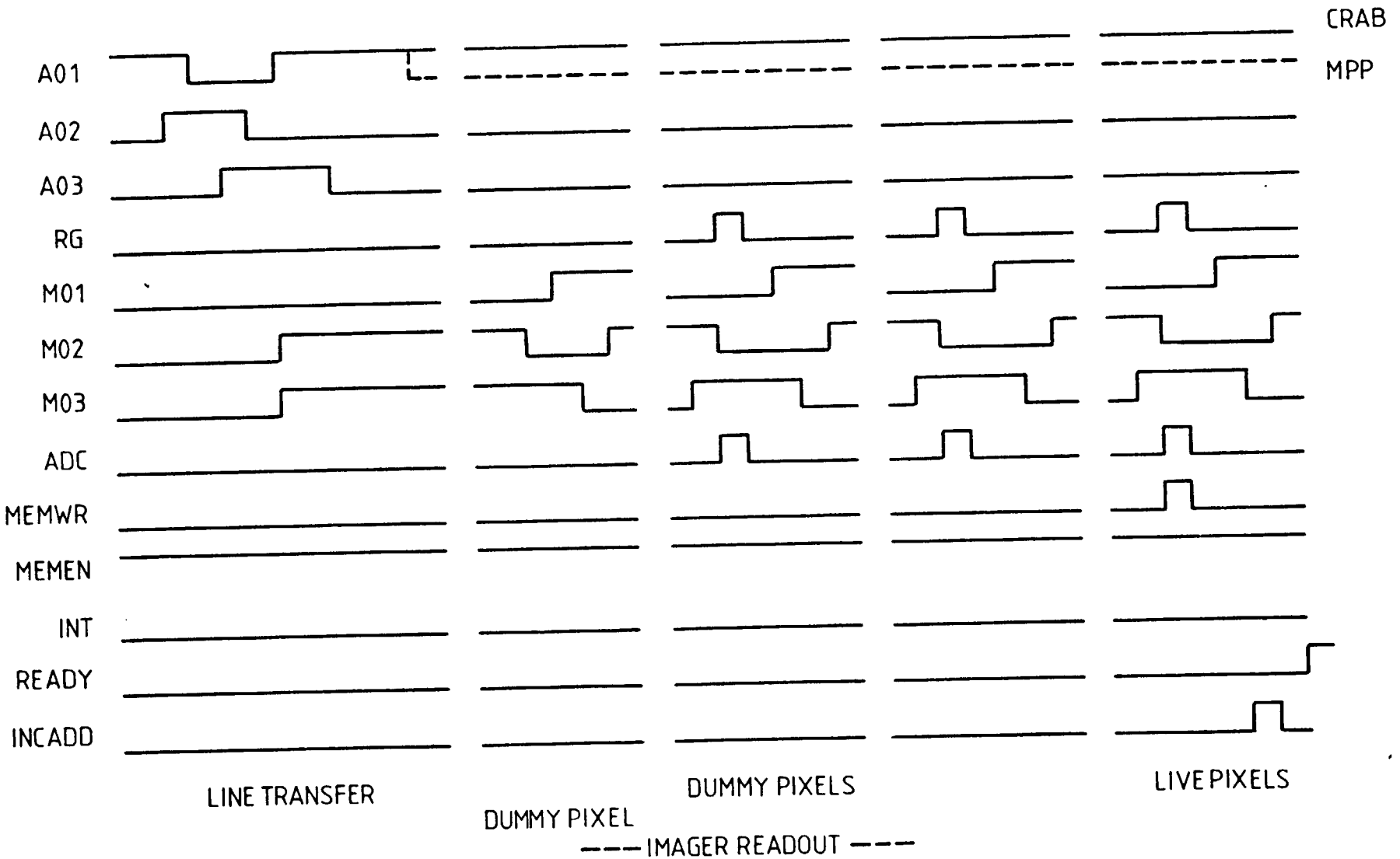

CRAB
MPP
A01
A02
A03
RG
M01
M02
M03
ADC
MEMWR
MEMEN
INT
READY
INCADD
LINE TRANSFER
DUMMY PIXEL
DUMMY PIXELS
LIVE PIXELS
IMAGER READOUT

FIG. 9D

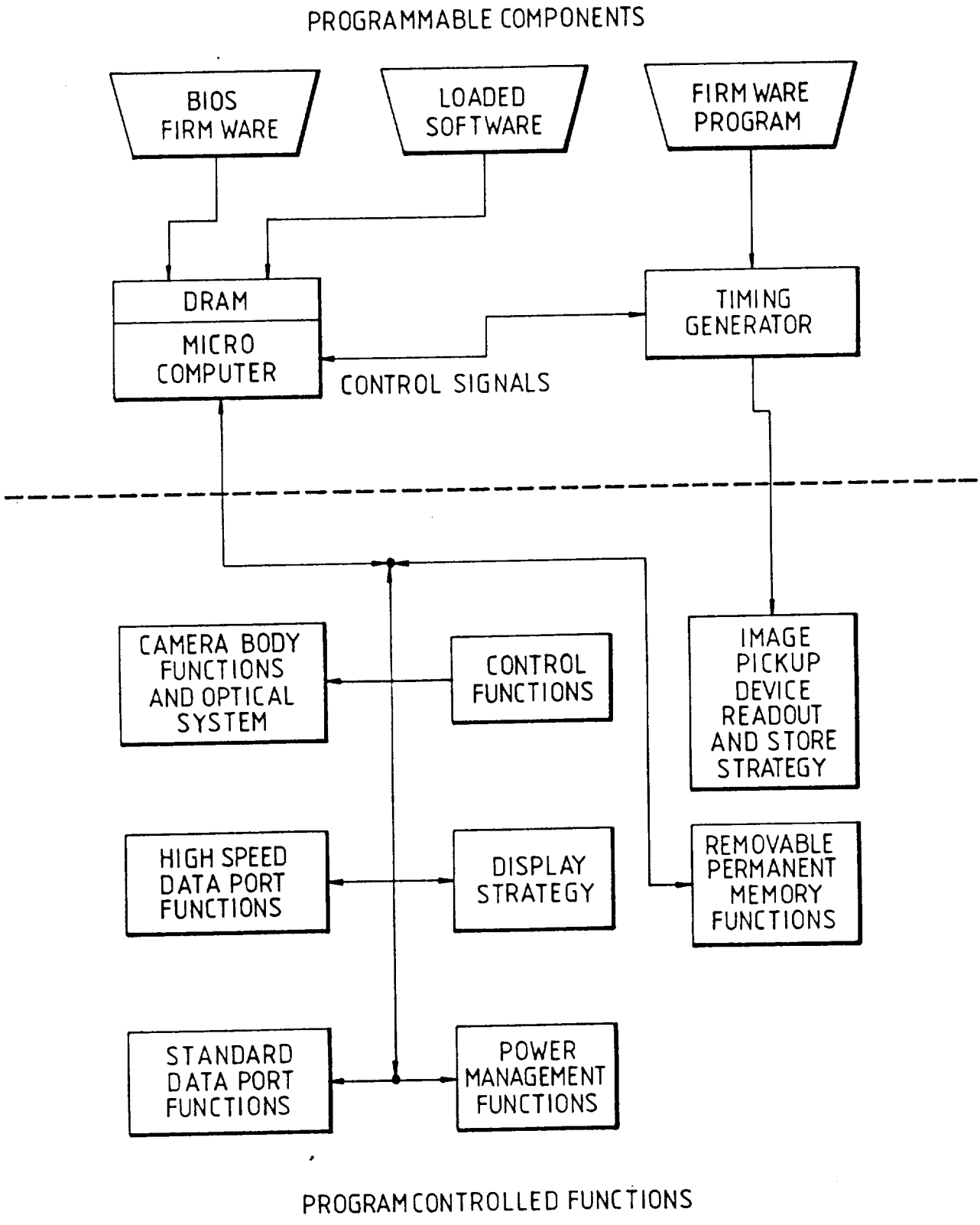

PROGRAMMABLE COMPONENTS
BIOS FIRM WARE
LOADED SOFTWARE
FIRM WARE PROGRAM
DRAM
MICRO COMPUTER
CONTROL SIGNALS
TIMING GENERATOR
CAMERA BODY FUNCTIONS AND OPTICAL SYSTEM
CONTROL FUNCTIONS
IMAGE PICKUP DEVICE READOUT AND STORE STRATEGY
HIGH SPEED DATA PORT FUNCTIONS
DISPLAY STRATEGY
REMOVABLE PERMANENT MEMORY FUNCTIONS
STANDARD DATA PORT FUNCTIONS
POWER MANAGEMENT FUNCTIONS
PROGRAM CONTROLLED FUNCTIONS

FIG.10

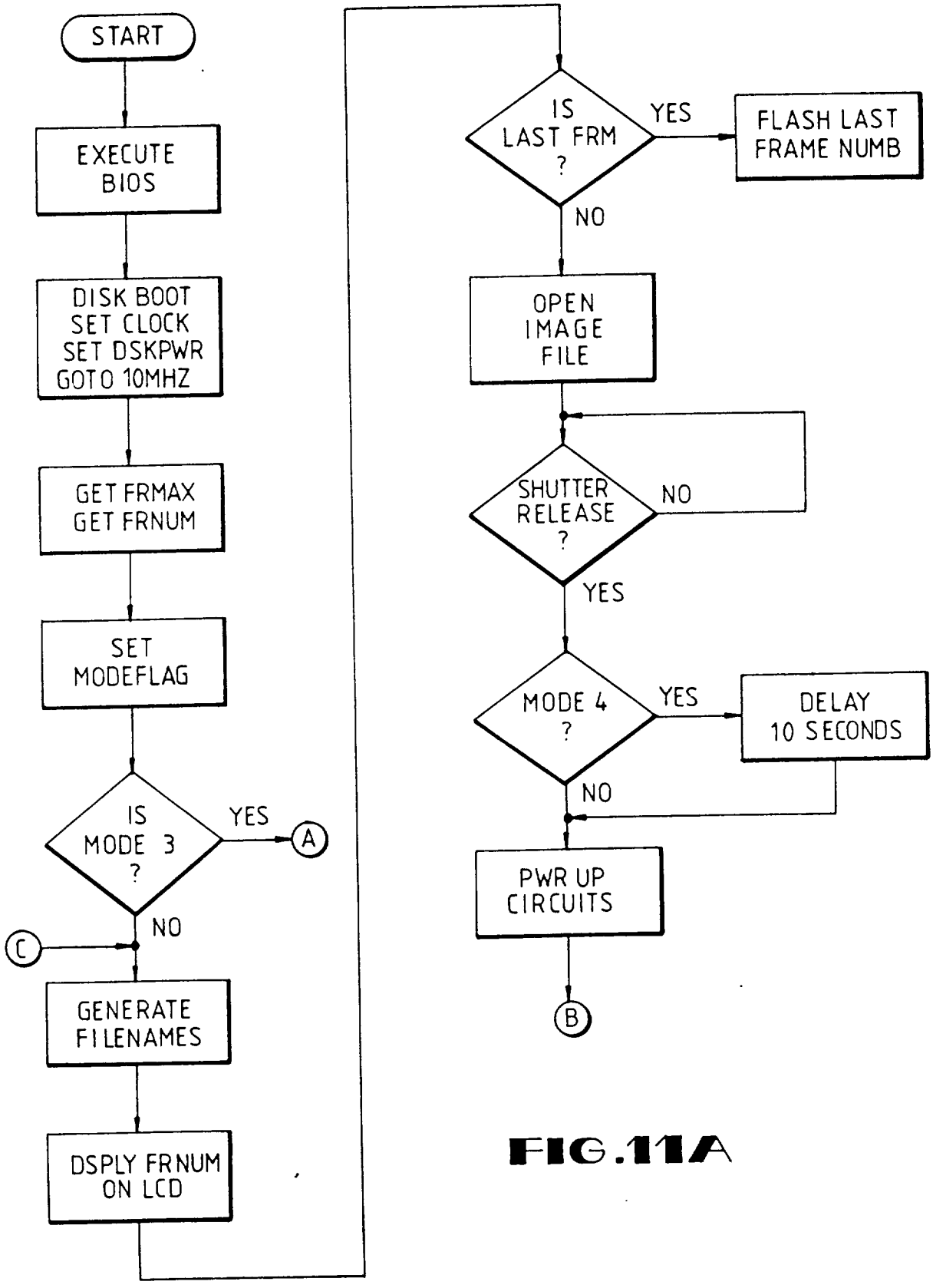

START
EXECUTE BIOS
DISK BOOT
SET CLOCK
SET DSKPWR
GOTO 10MHZ
GET FRMAX
GET FRNUM
SET MODEFLAG
IS MODE 3 ?
YES
A
NO
C
GENERATE FILENAMES
DSPLY FRNUM ON LCD
IS LAST FRM ?
YES
FLASH LAST FRAME NUMB
NO
OPEN IMAGE FILE
SHUTTER RELEASE ?
NO
YES
MODE 4 ?
YES
DELAY 10 SECONDS
NO
PWR UP CIRCUITS
B

FIG.11A

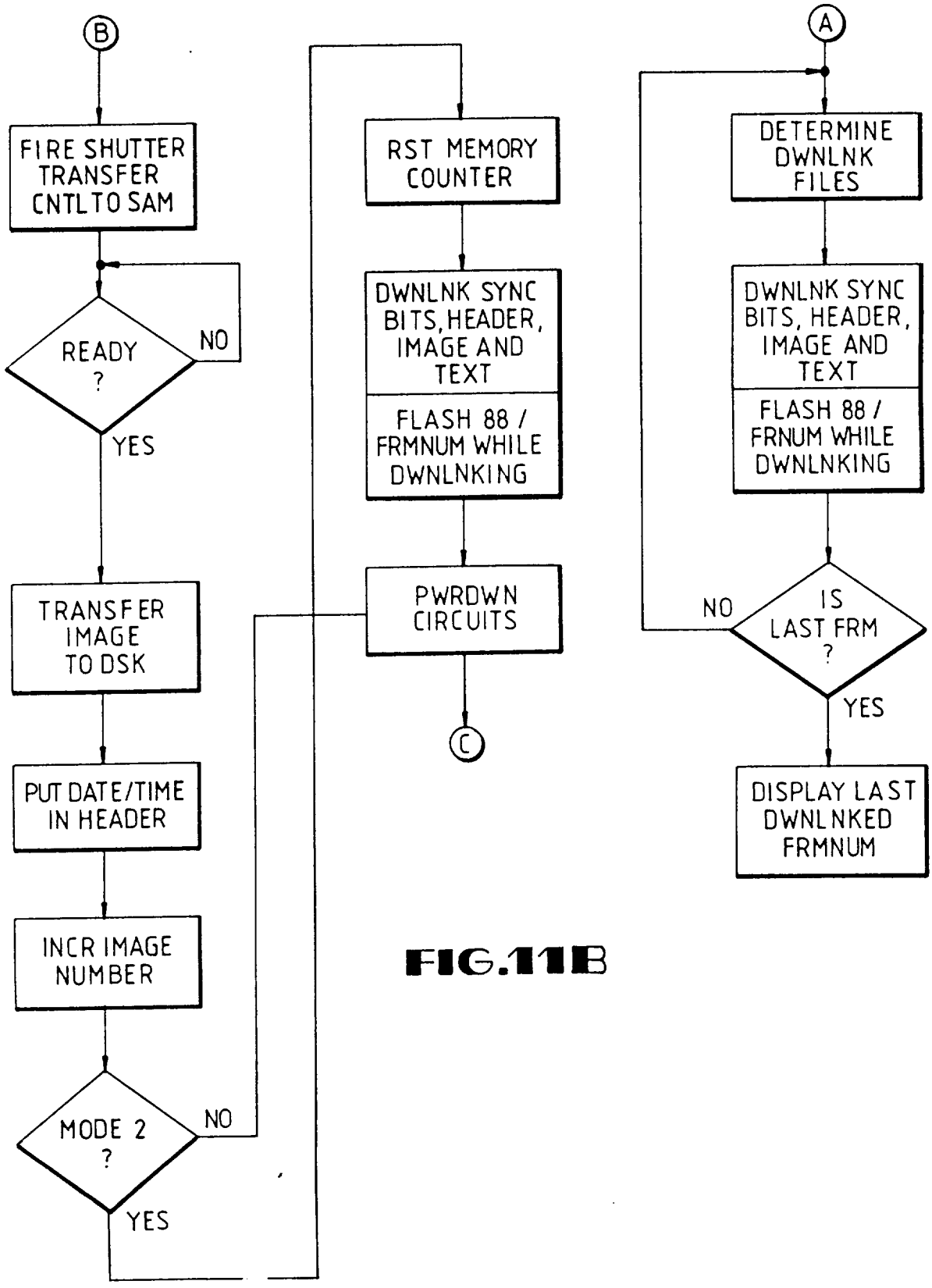

B
FIRE SHUTTER TRANSFER CNTL TO SAM
READY ?
NO
YES
TRANSFER IMAGE TO DSK
PUT DATE/TIME IN HEADER
INCR IMAGE NUMBER
MODE 2 ?
NO
YES
RST MEMORY COUNTER
DWNLNK SYNC BITS, HEADER, IMAGE AND TEXT
FLASH 88 / FRMNUM WHILE DWNLNKING
PWRDWN CIRCUITS
C
A
DETERMINE DWNLNK FILES
DWNLNK SYNC BITS, HEADER, IMAGE AND TEXT
FLASH 88 / FRNUM WHILE DWNLNKING
NO
IS LAST FRM ?
YES
DISPLAY LAST DWNLNKED FRMNUM

FIG.11B

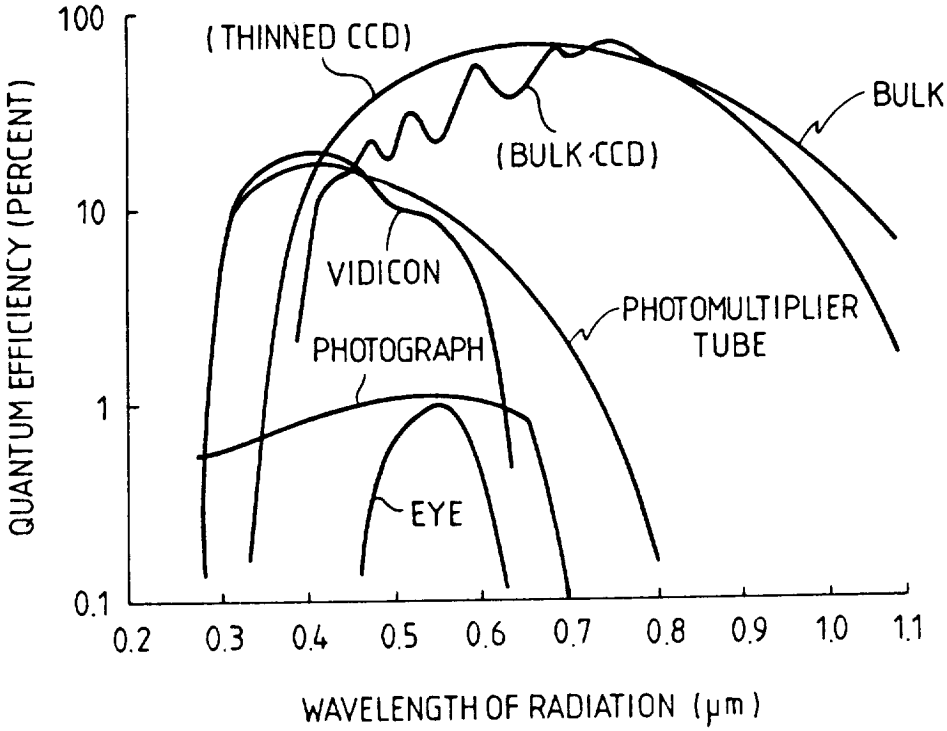

100
10
1
0.1
QUANTUM EFFICIENCY (PERCENT)
(THINNED CCD)
(BULK CCD)
BULK
VIDICON
PHOTOMULTIPLIER TUBE
PHOTOGRAPH
EYE
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
WAVELENGTH OF RADIATION (μm)

FIG.6

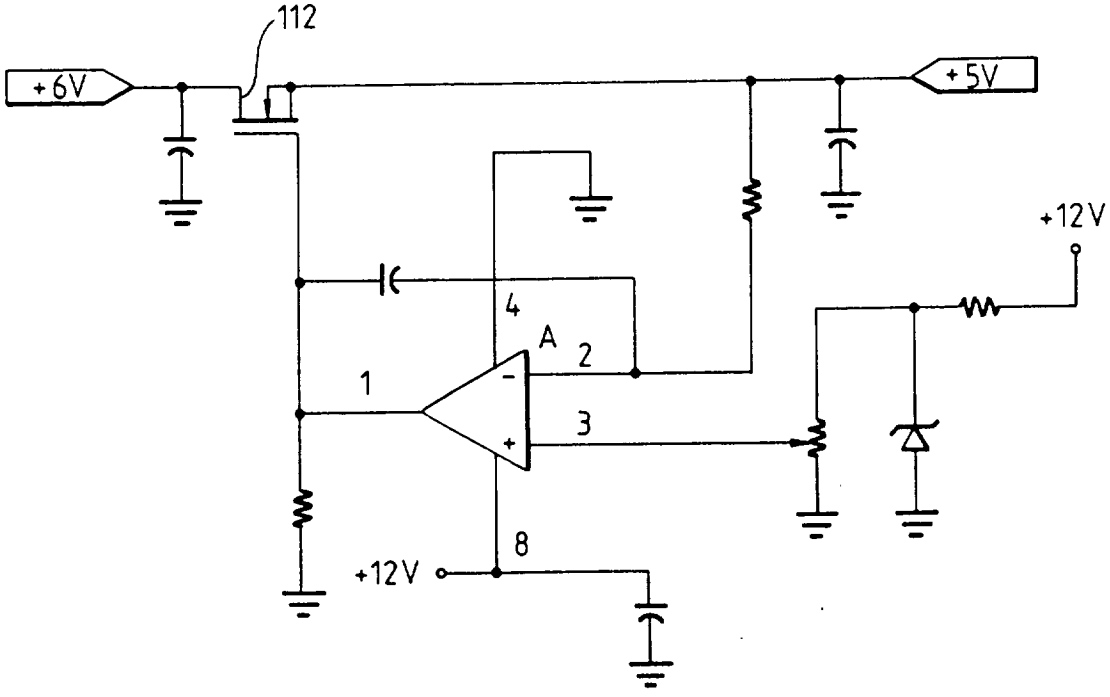
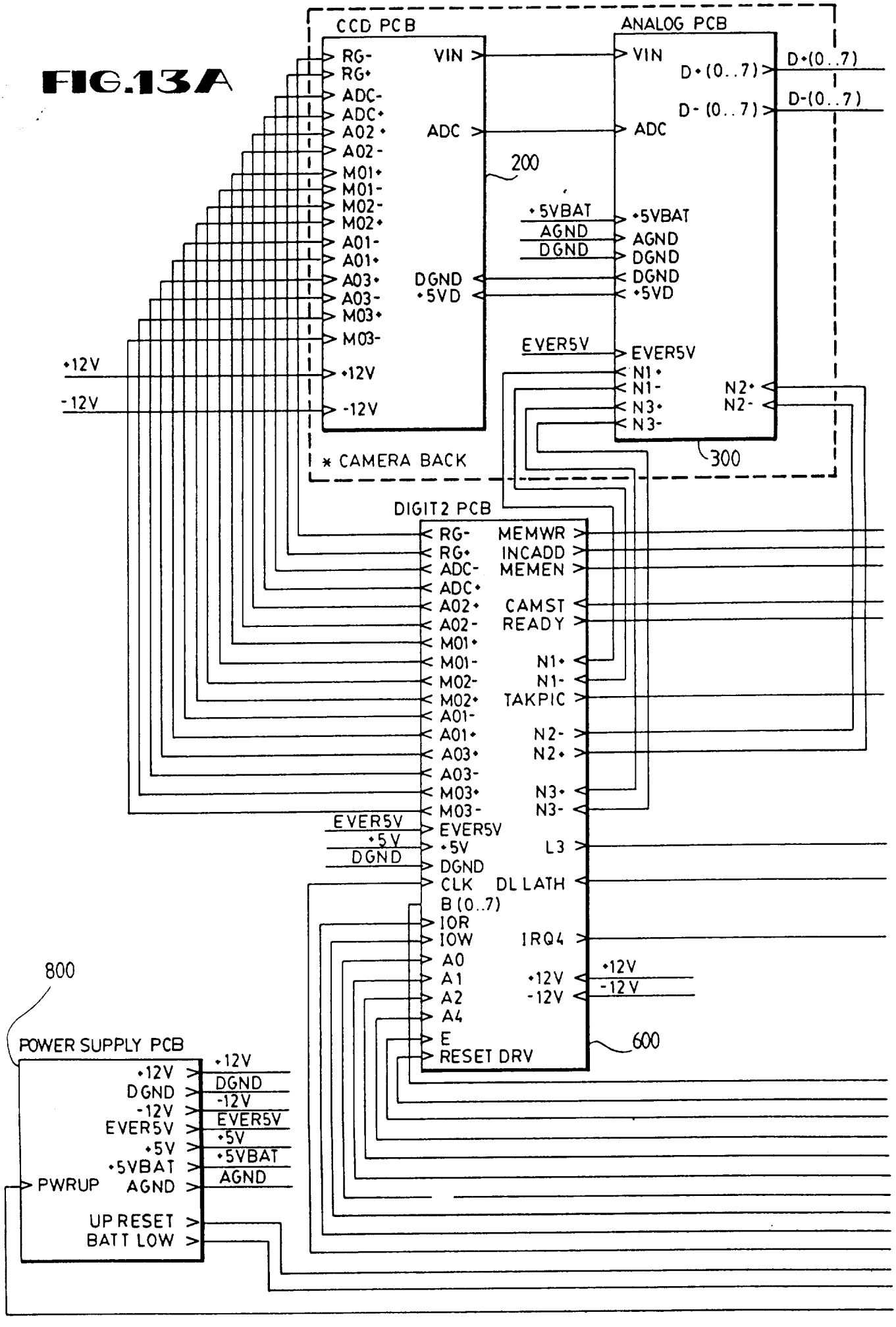

112
+6V
+5V
+12V
4
A
2
1
3
8
+12V

FIG.12

FIG.13A


CCD PCB
ANALOG PCB
RG-
RG+
ADC-
ADC+
A02+
A02-
M01+
M01-
M02-
M02+
A01-
A01+
A03+
A03-
M03+
M03-
+12V
-12V
VIN
ADC
DGND
+5VD
200
VIN
D+(0..7)
D-(0..7)
ADC
+5VBAT
AGND
DGND
+5VD
EVER5V
N1+
N1-
N3+
N3-
N2+
N2-
300
* CAMERA BACK
DIGIT2 PCB
MEMWR
INCADD
MEMEN
CAMST
READY
TAKPIC
L3
DL LATH
IRQ4
B(0..7)
IOR
IOW
A0
A1
A2
A4
E
RESET DRV
600
800
POWER SUPPLY PCB
PWRUP
UP RESET
BATT LOW

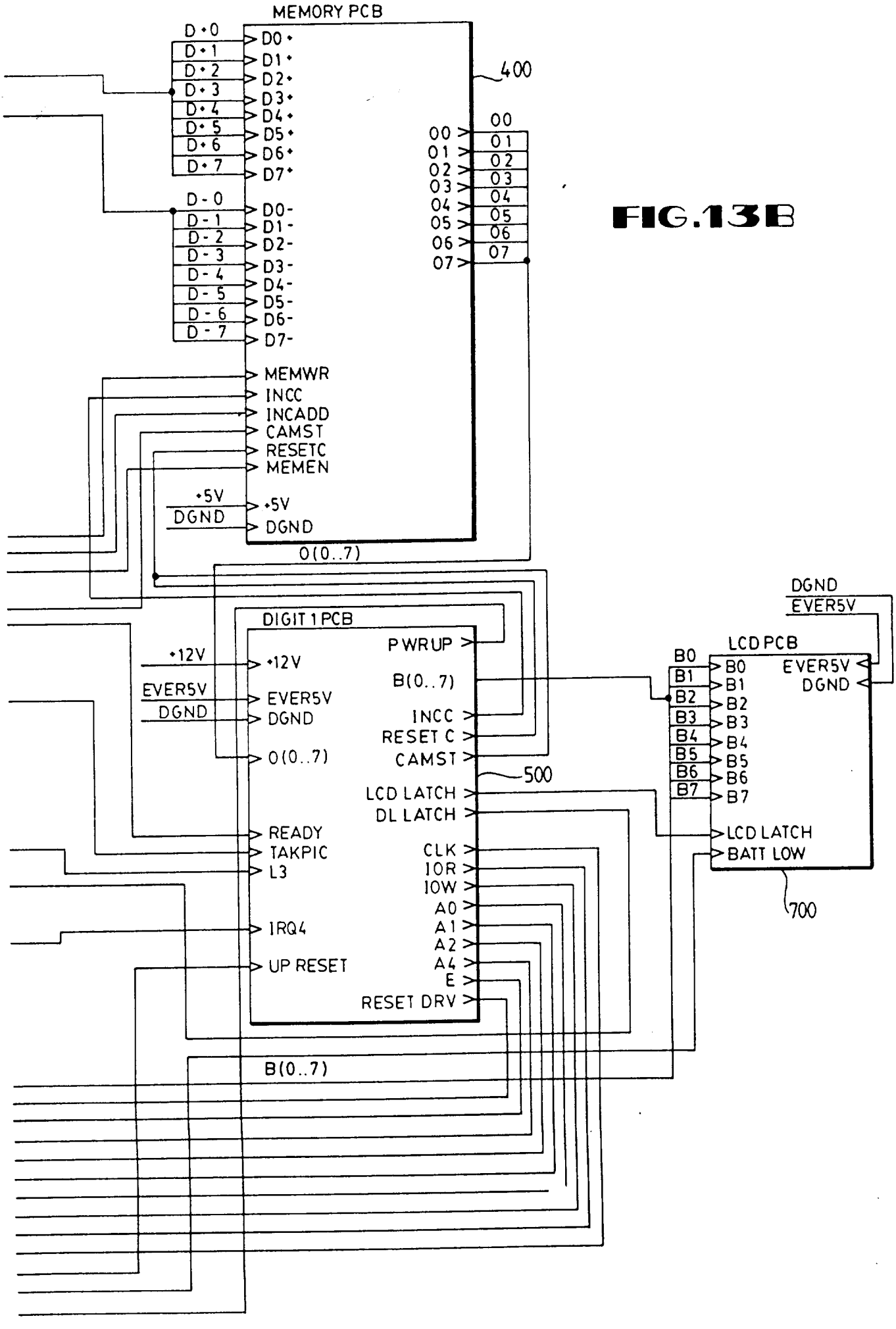

MEMORY PCB
D•0
D•1
D•2
D•3
D•4
D•5
D•6
D•7
D0•
D1•
D2•
D3•
D4•
D5•
D6•
D7•
400
00
01
02
03
04
05
06
07
D-0
D-1
D-2
D-3
D-4
D-5
D-6
D-7
D0-
D1-
D2-
D3-
D4-
D5-
D6-
D7-
MEMWR
INCC
INCADD
CAMST
RESETC
MEMEN
•5V
DGND
•5V
DGND
O(0..7)
DIGIT 1 PCB
•12V
•12V
EVER5V
DGND
EVER5V
DGND
O(0..7)
PWRUP
B(0..7)
INCC
RESET C
CAMST
500
LCD LATCH
DL LATCH
READY
TAKPIC
L3
IRQ4
UP RESET
CLK
IOR
IOW
A0
A1
A2
A4
E
RESET DRV
B(0..7)
DGND
EVER5V
LCD PCB
B0
B1
B2
B3
B4
B5
B6
B7
EVER5V
DGND
LCD LATCH
BATT LOW
700

FIG.13B

FIG.14A

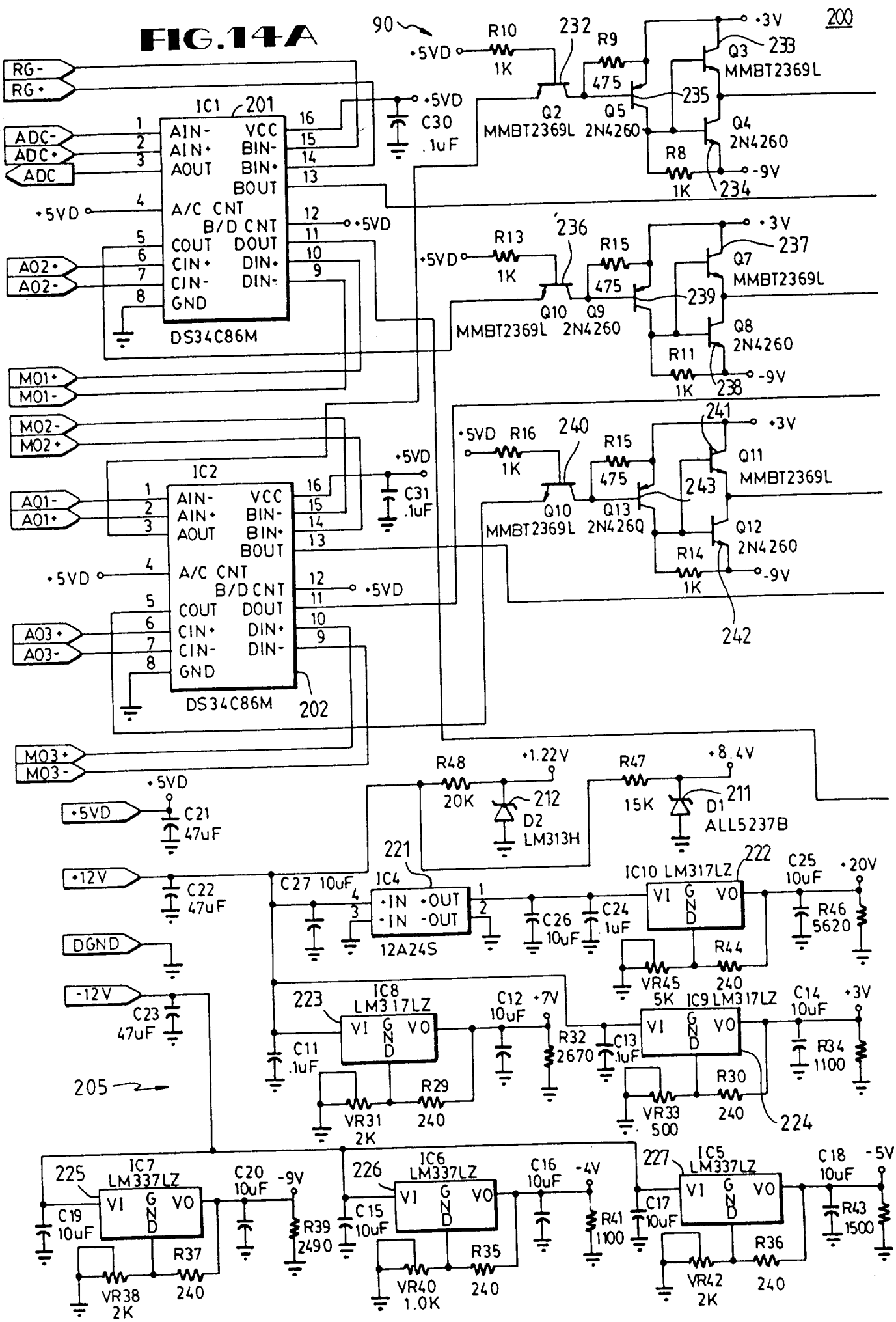
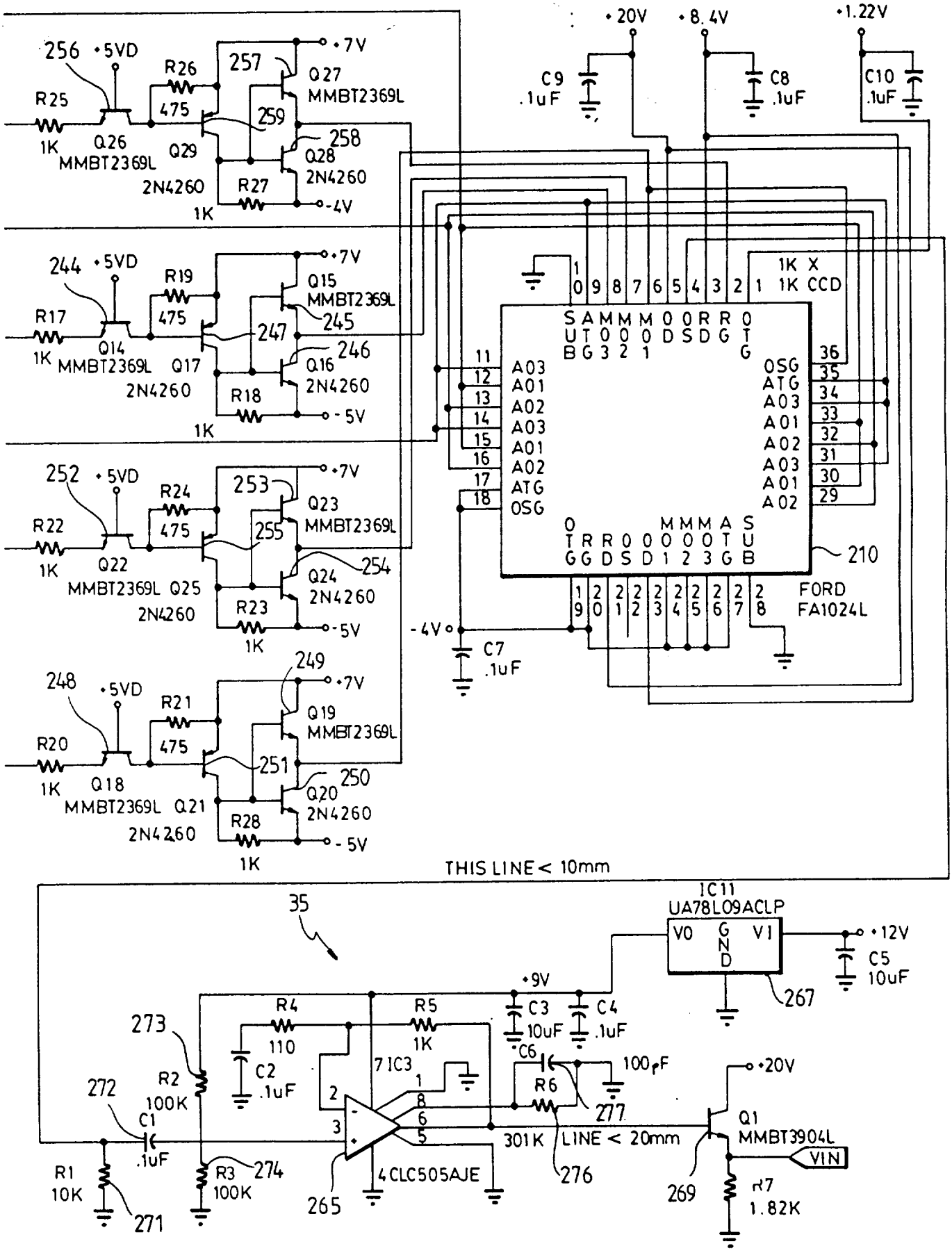

90
200
RG-
RG+
ADC-
ADC+
ADC
IC1
201
AIN-
AIN+
AOUT
VCC
BIN-
BIN+
BOUT
A/C CNT
B/D CNT
COUT
DOUT
CIN+
DIN+
CIN-
DIN-
GND
DS34C86M
+5VD
C30
.1uF
R10
1K
232
R9
475
Q2
MMBT2369L
Q5
2N4260
Q3
MMBT2369L
233
235
Q4
2N4260
R8
1K
234
+3V
-9V
A02+
A02-
R13
236
R15
Q10
MMBT2369L
Q9
2N4260
Q7
MMBT2369L
237
239
Q8
2N4260
R11
1K
238
M01+
M01-
M02-
M02+
IC2
C31
.1uF
R16
240
241
Q11
MMBT2369L
243
Q10
MMBT2369L
Q13
2N4260
Q12
2N4260
R14
1K
242
A01-
A01+
A03+
A03-
202
M03+
M03-
R48
20K
+1.22V
212
D2
LM313H
R47
15K
+8.4V
211
D1
ALL5237B
+12V
-12V
DGND
C21
47uF
C22
47uF
C23
47uF
205
C27 10uF
221
IC4
+IN +OUT
-IN -OUT
12A24S
C26
10uF
C24
1uF
IC10 LM317LZ
222
VI GND VO
C25
10uF
+20V
R46
5620
R44
240
VR45
5K
223
IC8
LM317LZ
C11
.1uF
C12
10uF
+7V
R32
2670
C13
.1uF
IC9 LM317LZ
C14
10uF
+3V
R34
1100
R29
VR31
2K
R30
VR33
500
224
225
IC7
LM337LZ
C19
10uF
C20
10uF
-9V
R39
2490
R37
VR38
2K
240
226
IC6
LM337LZ
C15
10uF
C16
10uF
-4V
R41
1100
R35
VR40
1.0K
240
227
IC5
LM337LZ
C17
10uF
C18
10uF
-5V
R43
1500
R36
VR42
2K
240

FIG.14B


+20V
+8.4V
+1.22V
C9 .1uF
C8 .1uF
C10 .1uF
256 +5VD
R26
257
Q27 MMBT2369L
+7V
R25
475
259
1K
Q26 MMBT2369L
Q29
258
Q28 2N4260
2N4260
R27
-4V
1K
244 +5VD
R19
Q15 MMBT2369L
R17
475
247
245
1K
Q14 MMBT2369L
Q17
246
Q16 2N4260
2N4260
R18
-5V
1K
1K X 1K CCD
SAMMM00RR0 UT0001DSDGT BG321 G
OSG ATG A03 A01 A02 A03 A01 A02
A03 A01 A02 A03 A01 A02 ATG OSG
OTRR00000ASU GGDSD1234GB
210
FORD FA1024L
252 +5VD
R24
253
Q23 MMBT2369L
R22
475
255
254
1K
Q22 MMBT2369L Q25
Q24 2N4260
2N4260
R23
-5V
1K
-4V
C7 .1uF
249
248 +5VD
R21
Q19 MMBT2369L
R20
475
251
250
1K
Q18 MMBT2369L Q21
Q20 2N4260
2N4260
R28
-5V
1K
THIS LINE < 10mm
35
IC11 UA78L09ACLP
VO GND VI
+12V
C5 10uF
267
+9V
R4
R5
C3 10uF
C4 .1uF
273
110
1K
C6
100pF
C2 .1uF
7IC3
R2 100K
272
R6
+20V
C1 .1uF
277
Q1 MMBT3904L
VIN
301K
LINE < 20mm
276
R1 10K
R3 100K
274
4CLC505AJE
265
269
R7 1.82K
271

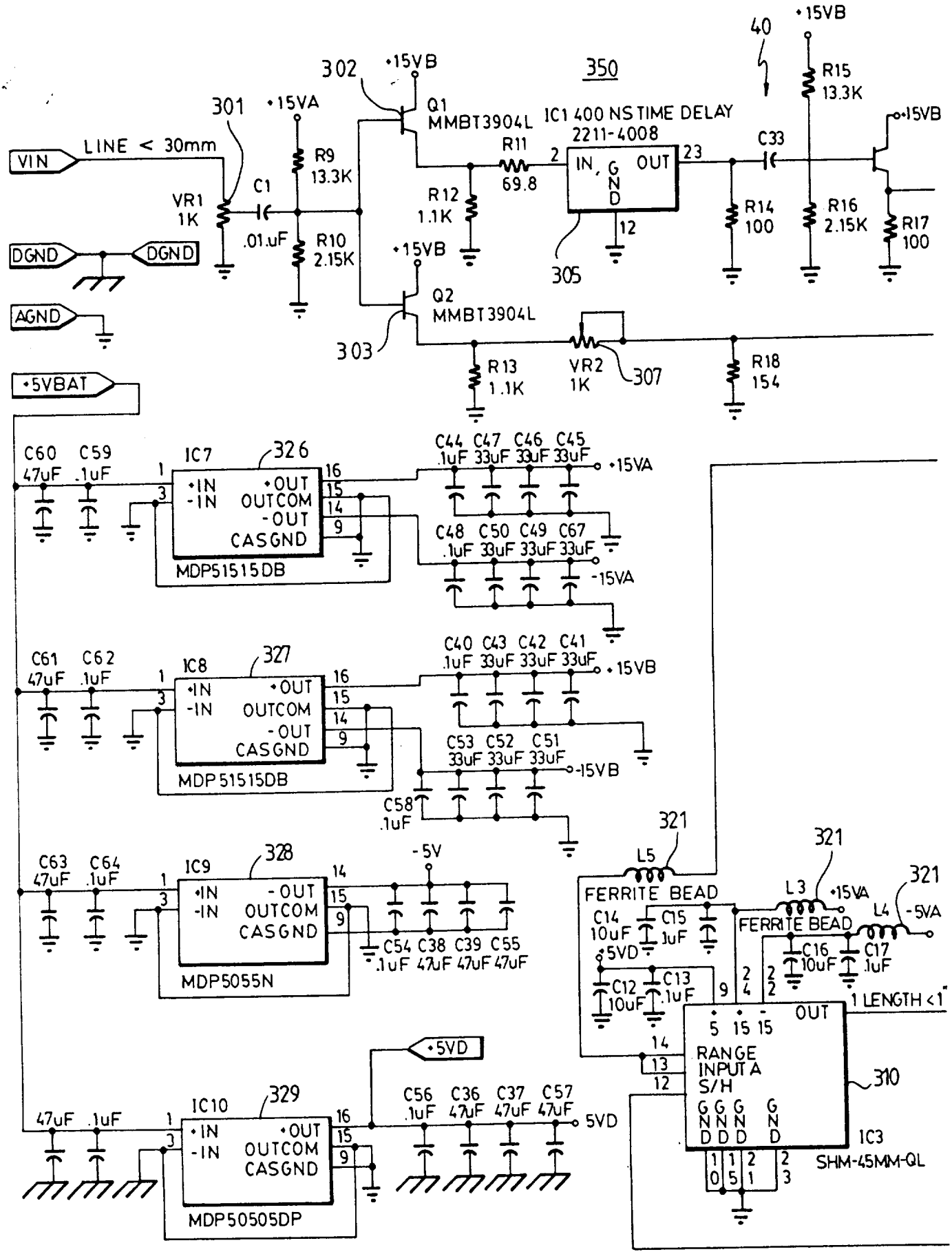


FIG.16A

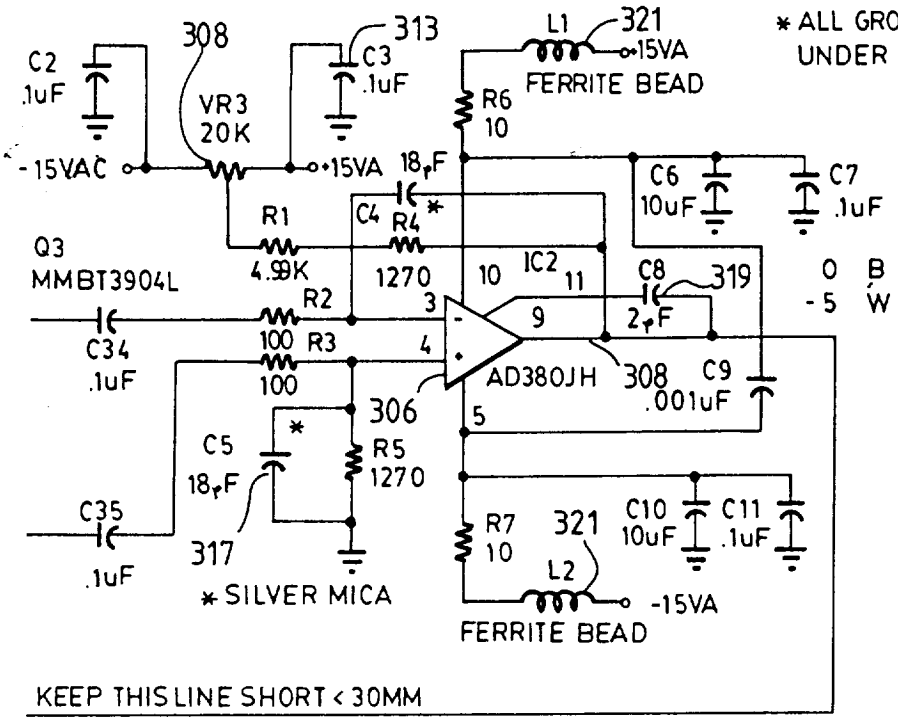
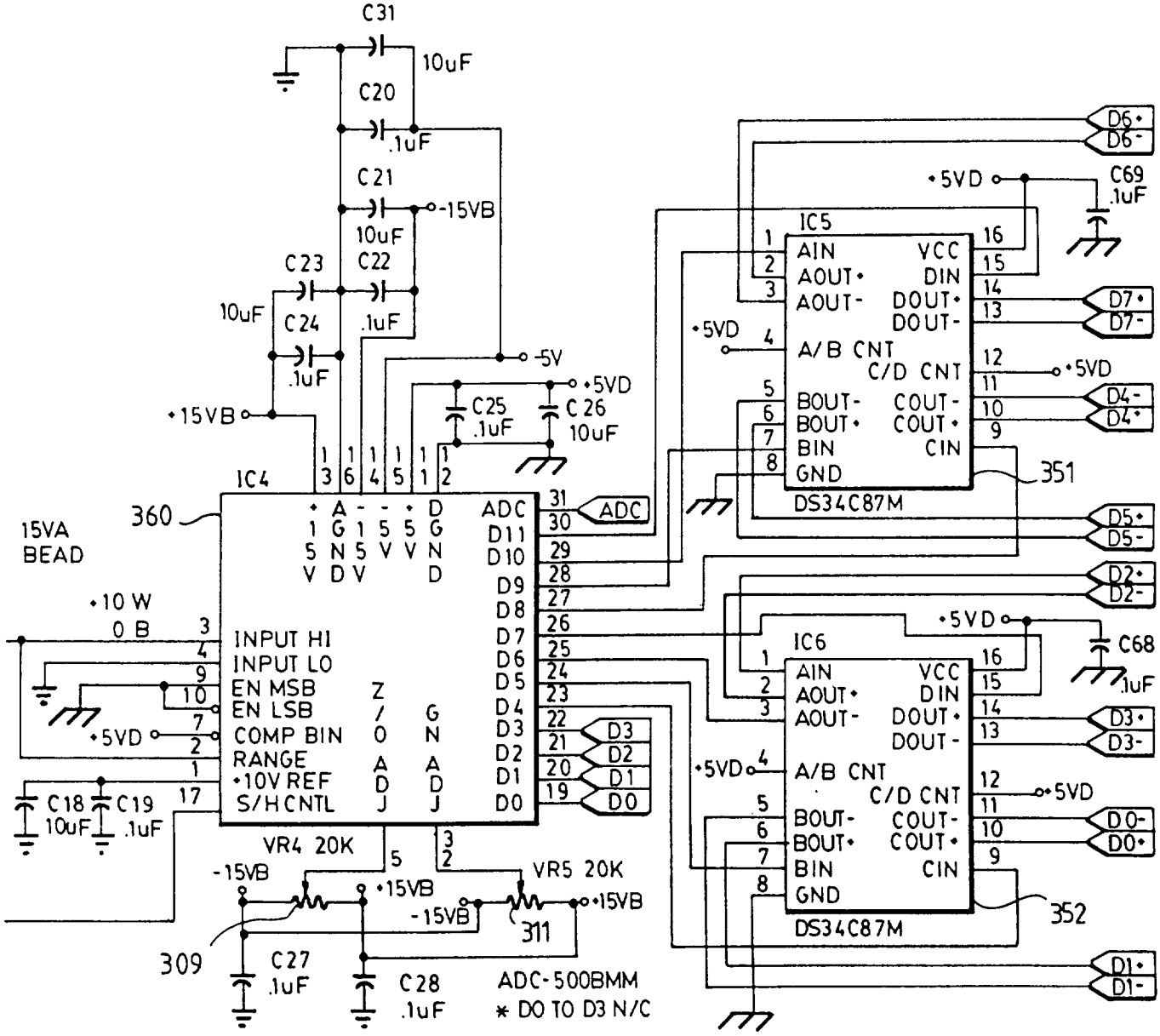

* ALL GROUNDS CONNECTED TO GND PLANE UNDER A/D AT ONE POINT
C2 .1uF
308
VR3 20K
313
C3 .1uF
L1
321
+15VA
FERRITE BEAD
R6 10
-15VAC
+15VA
18pF
C6 10uF
C7 .1uF
R1 4.99K
C4 *
R4 1270
Q3 MMBT3904L
IC2
C8
319
2pF
0 B
-5 W
R2 100
C34 .1uF
R3 100
AD380JH
308
C9 .001uF
306
C5 18pF *
R5 1270
C35 .1uF
317
* SILVER MICA
R7 10
321
L2
C10 10uF
C11 .1uF
-15VA
FERRITE BEAD
KEEP THIS LINE SHORT < 30MM

FIG.16B


C31 10uF
C20 .1uF
C21 10uF
-15VB
C23 10uF
C22 .1uF
C24 .1uF
-5V
+5VD
+15VB
C25 .1uF
C26 10uF
IC4
360
15VA BEAD
+10 W
0 B
INPUT HI
INPUT LO
EN MSB
EN LSB
COMP BIN
RANGE
+10V REF
S/H CNTL
ADC
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
C18 10uF
C19 .1uF
VR4 20K
VR5 20K
-15VB
+15VB
309
311
C27 .1uF
C28 .1uF
ADC-500BMM
* D0 TO D3 N/C
IC5
AIN
AOUT+
AOUT-
A/B CNT
BOUT-
BOUT+
BIN
GND
VCC
DIN
DOUT+
DOUT-
C/D CNT
COUT-
COUT+
CIN
DS34C87M
351
C69 .1uF
D6+
D6-
D7+
D7-
D4-
D4+
D5+
D5-
IC6
352
C68 .1uF
D3+
D3-
D0-
D0+
D1+
D1-

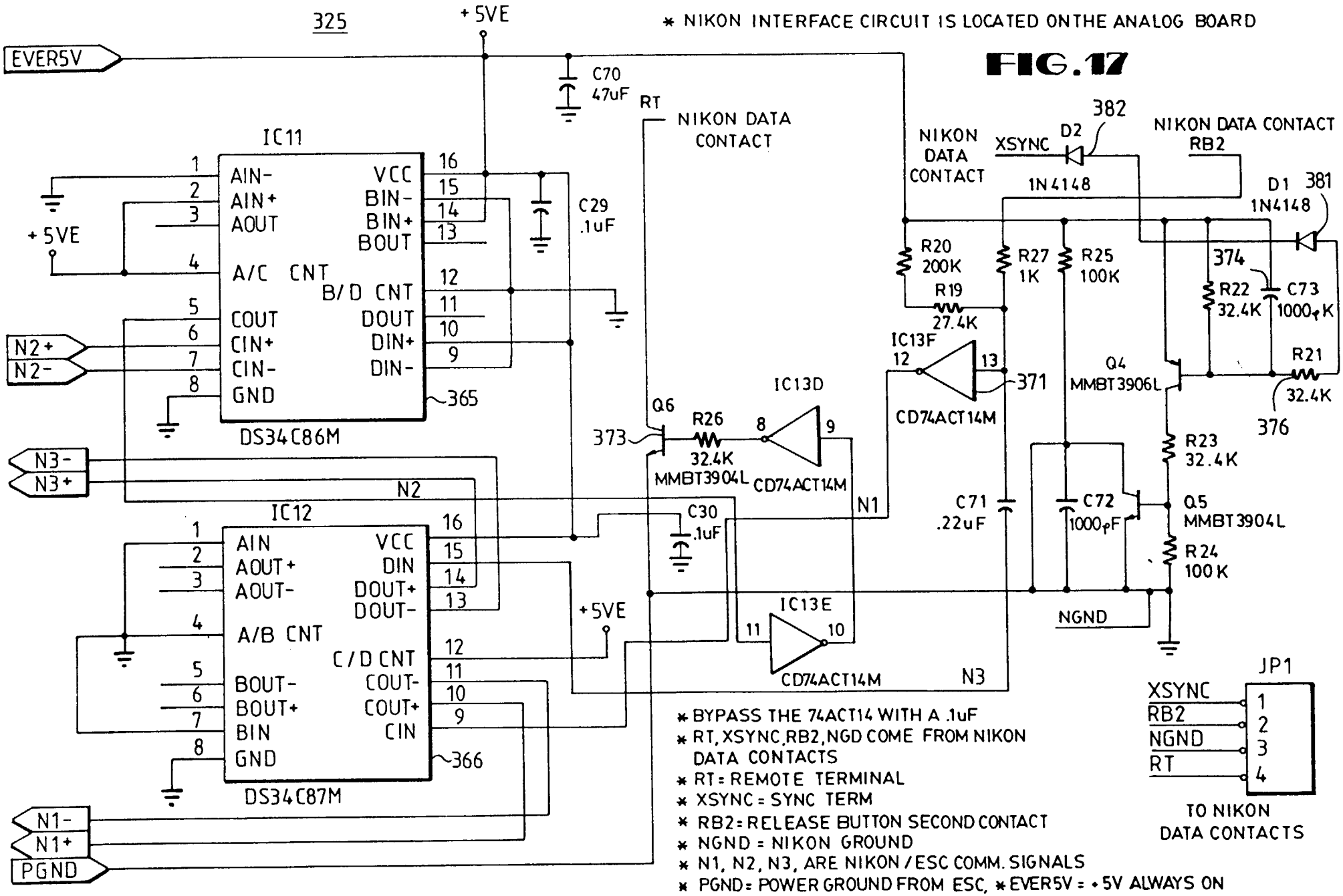

325
+5VE
* NIKON INTERFACE CIRCUIT IS LOCATED ONTHE ANALOG BOARD
EVER5V
C70
47uF
RT
NIKON DATA CONTACT
382
NIKON DATA CONTACT
XSYNC
D2
1N4148
NIKON DATA CONTACT
RB2
D1
381
1N4148
IC11
AIN-
AIN+
AOUT
A/C CNT
B/D CNT
COUT
CIN+
CIN-
GND
VCC
BIN-
BIN+
BOUT
DOUT
DIN+
DIN-
365
DS34C86M
C29
.1uF
+5VE
N2+
N2-
N3-
N3+
R20
200K
R19
27.4K
R27
1K
R25
100K
374
R22
32.4K
C73
1000pF
R21
32.4K
376
IC13F
CD74ACT14M
371
Q4
MMBT3906L
IC13D
Q6
373
R26
32.4K
MMBT3904L
CD74ACT14M
N2
N1
R23
32.4K
C71
.22uF
C72
1000pF
Q5
MMBT3904L
R24
100K
IC12
AIN
AOUT+
AOUT-
A/B CNT
C/D CNT
BOUT-
BOUT+
BIN
GND
VCC
DIN
DOUT+
DOUT-
COUT-
COUT+
CIN
366
DS34C87M
C30
.1uF
+5VE
IC13E
CD74ACT14M
N3
NGND
JP1
XSYNC
RB2
NGND
RT
TO NIKON DATA CONTACTS
N1-
N1+
PGND
* BYPASS THE 74ACT14 WITH A .1uF
* RT, XSYNC, RB2, NGD COME FROM NIKON DATA CONTACTS
* RT = REMOTE TERMINAL
* XSYNC = SYNC TERM
* RB2 = RELEASE BUTTON SECOND CONTACT
* NGND = NIKON GROUND
* N1, N2, N3, ARE NIKON / ESC COMM. SIGNALS
* PGND = POWER GROUND FROM ESC, * EVER5V = +5V ALWAYS ON

FIG. 17

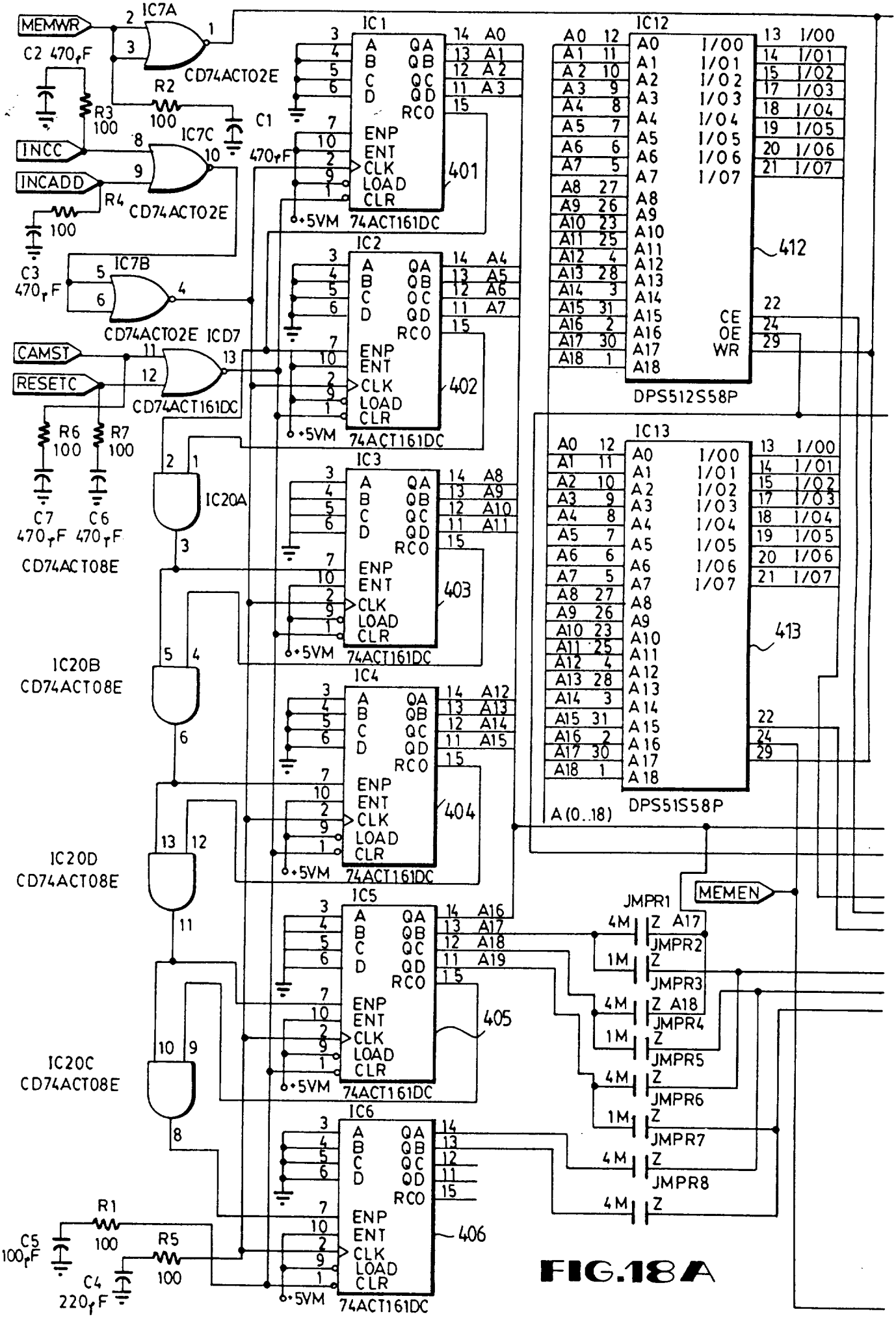

MEMWR
IC7A
CD74ACT02E
C2 470pF
R2
R3 100
100
C1
470pF
INCC
IC7C
INCADD
R4
100
CD74ACT02E
C3
470pF
IC7B
CD74ACT02E
IC7D
CAMST
RESETC
CD74ACT161DC
R6 100
R7 100
C7 470pF
C6 470pF
CD74ACT08E
IC20A
IC20B
CD74ACT08E
IC20D
CD74ACT08E
IC20C
CD74ACT08E
R1
100
C5 100pF
R5
100
C4 220pF
IC1
IC2
IC3
IC4
IC5
IC6
ENP
ENT
CLK
LOAD
CLR
RCO
+5VM
74ACT161DC
401
402
403
404
405
406
IC12
IC13
DPS512S58P
DPS51S58P
412
413
CE
OE
WR
A(0..18)
MEMEN
JMPR1
JMPR2
JMPR3
JMPR4
JMPR5
JMPR6
JMPR7
JMPR8
4M
1M

FIG.18A

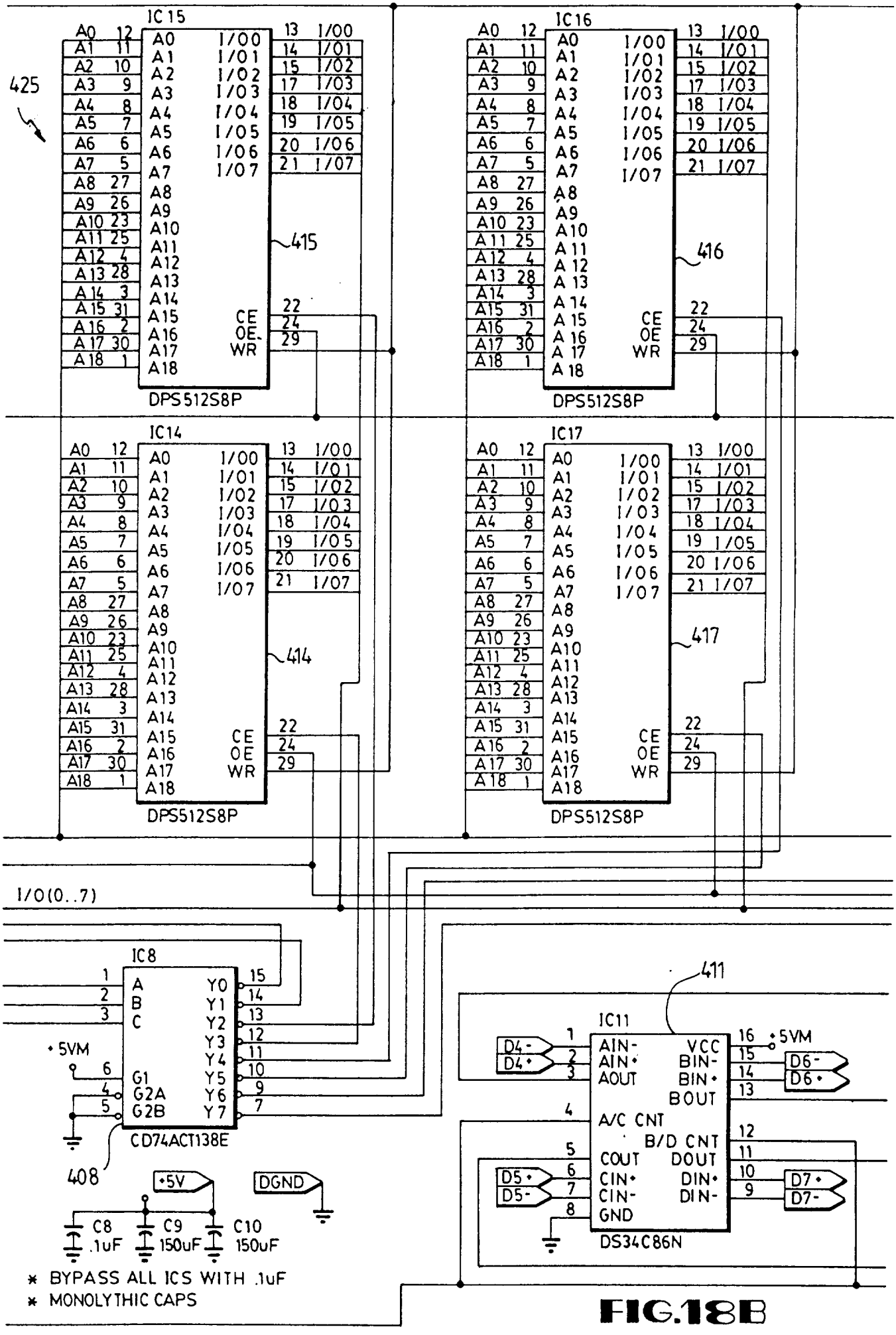

IC15
IC16
IC14
IC17
425
415
416
414
417
DPS512S8P
I/O(0..7)
IC8
CD74ACT138E
408
IC11
411
DS34C86N
+5VM
+5V
DGND
C8 .1uF
C9 150uF
C10 150uF
* BYPASS ALL ICS WITH .1uF
* MONOLYTHIC CAPS

FIG.18B

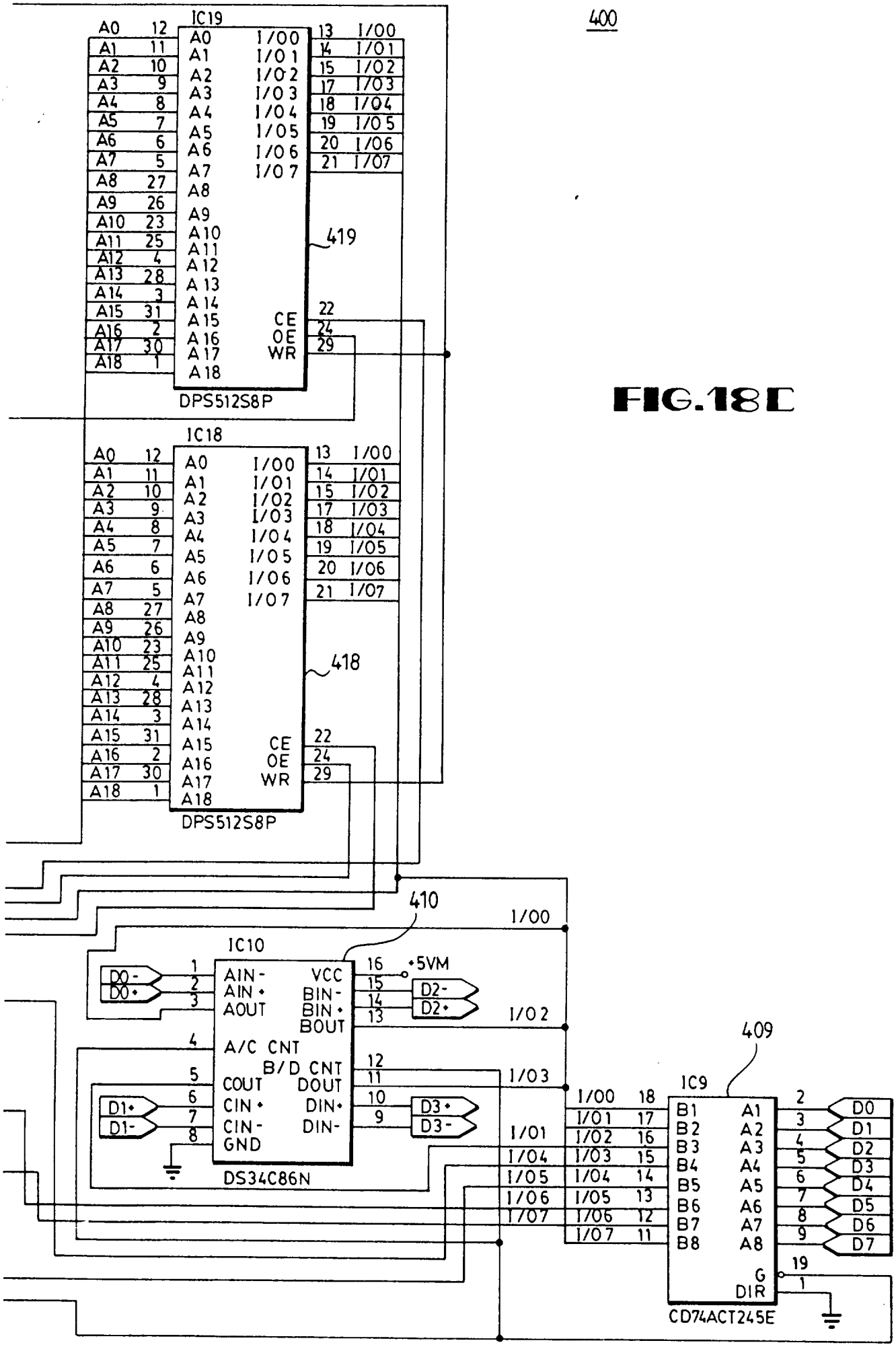
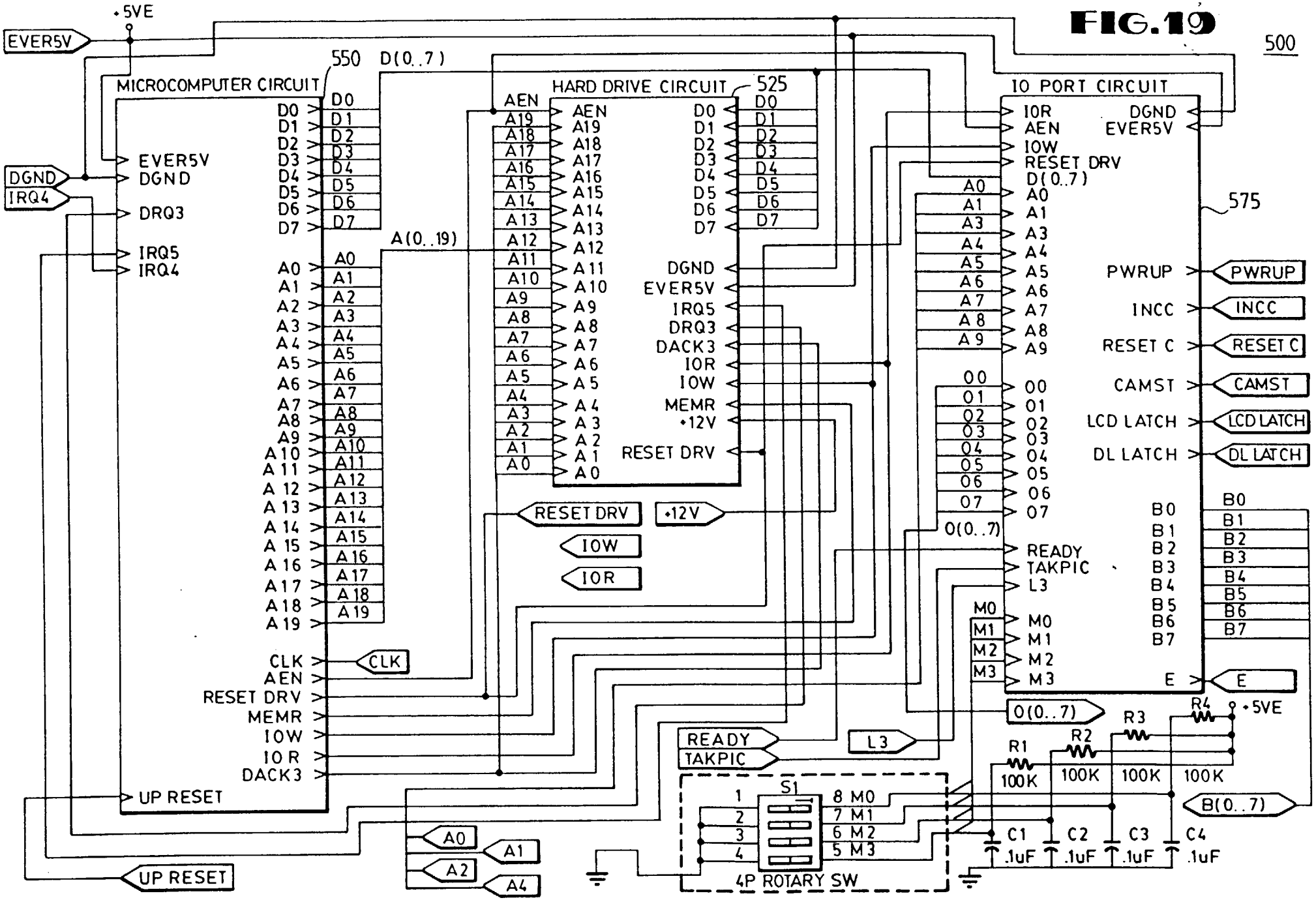

400
IC19
A0 12
A1 11
A2 10
A3 9
A4 8
A5 7
A6 6
A7 5
A8 27
A9 26
A10 23
A11 25
A12 4
A13 28
A14 3
A15 31
A16 2
A17 30
A18 1
A0 I/00
A1 I/01
A2 I/02
A3 I/03
A4 I/04
A5 I/05
A6 I/06
A7 I/07
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
CE
OE
WR
13 I/00
14 I/01
15 I/02
17 I/03
18 I/04
19 I/05
20 I/06
21 I/07
22
24
29
419
DPS512S8P
IC18
418
DPS512S8P
410
IC10
AIN-
AIN+
AOUT
VCC
BIN-
BIN+
BOUT
A/C CNT
B/D CNT
COUT
DOUT
CIN+
DIN+
CIN-
DIN-
GND
D0-
D0+
D1+
D1-
D2-
D2+
D3+
D3-
+5VM
DS34C86N
409
IC9
B1
B2
B3
B4
B5
B6
B7
B8
A1
A2
A3
A4
A5
A6
A7
A8
D0
D1
D2
D3
D4
D5
D6
D7
G
DIR
CD74ACT245E

FIG.18C

FIG.19


500
+5VE
EVER5V
550
D(0..7)
MICROCOMPUTER CIRCUIT
HARD DRIVE CIRCUIT
525
IO PORT CIRCUIT
575
DGND
IRQ4
DRQ3
IRQ5
A(0..19)
AEN
RESET DRV
+12V
IOW
IOR
MEMR
CLK
READY
TAKPIC
L3
UP RESET
A0
A1
A2
A4
S1
4P ROTARY SW
R1
R2
R3
R4
100K
C1
C2
C3
C4
.1uF
PWRUP
INCC
RESET C
CAMST
LCD LATCH
DL LATCH
B(0..7)
O(0..7)

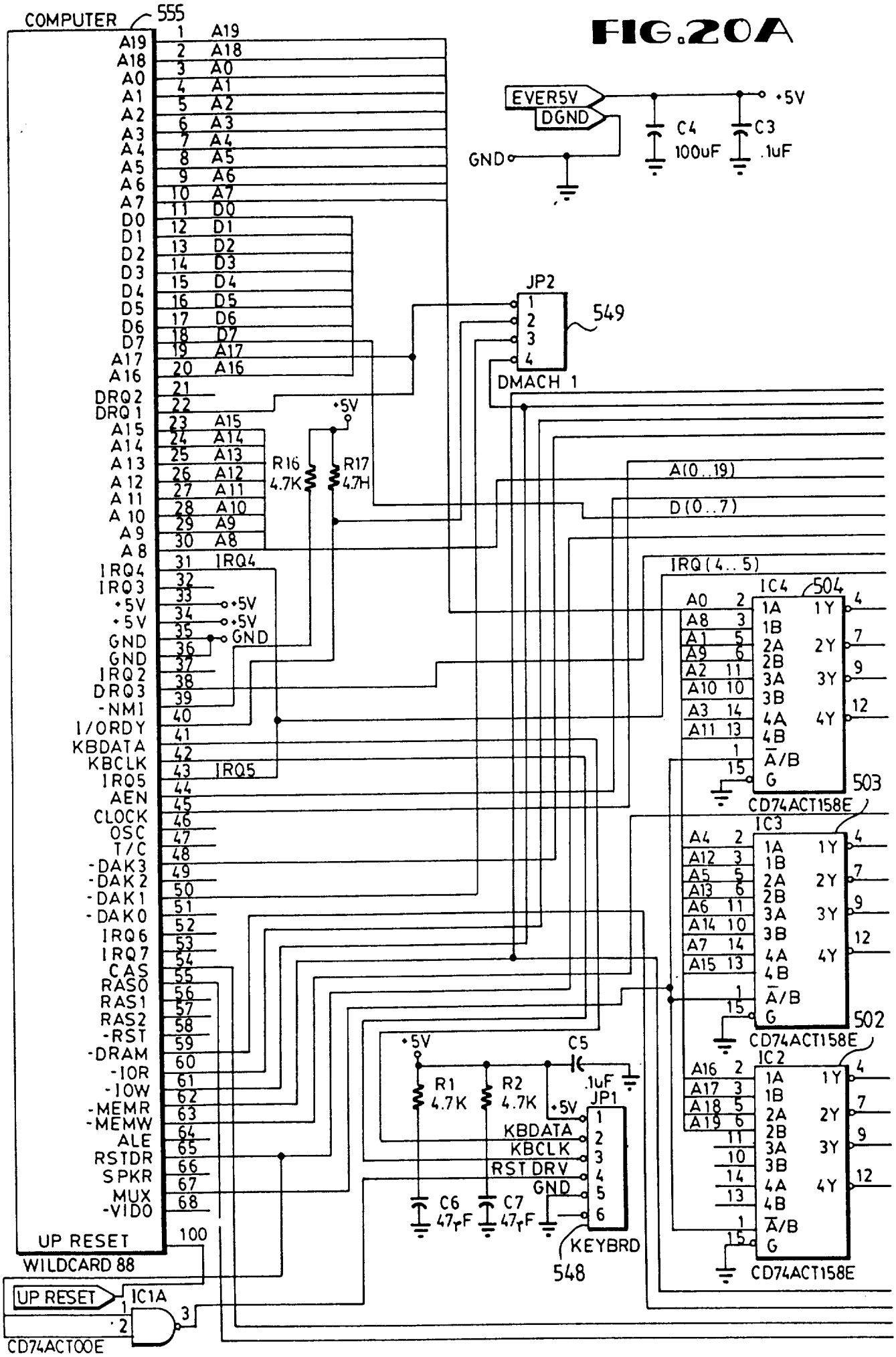
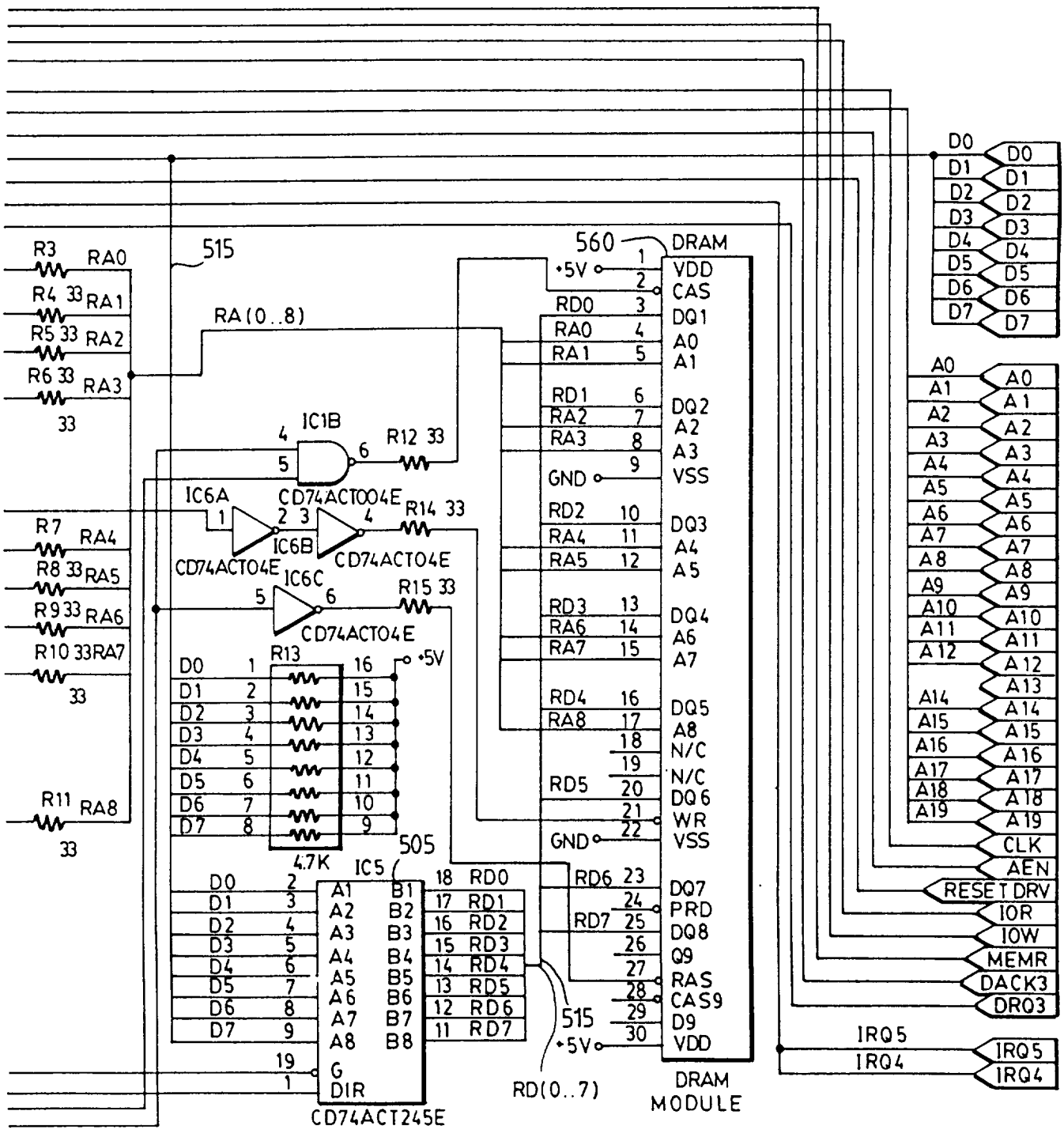


FIG.20A
COMPUTER
555
EVER5V
DGND
GND
+5V
C4
100uF
C3
.1uF
JP2
549
DMACH 1
+5V
R16
4.7K
R17
4.7H
A(0..19)
D(0..7)
IRQ(4..5)
IC4
504
CD74ACT158E
IC3
503
CD74ACT158E
IC2
502
CD74ACT158E
C5
.1uF
R1
4.7K
R2
4.7K
JP1
KBDATA
KBCLK
RST DRV
GND
KEYBRD
548
C6
47pF
C7
47pF
UP RESET
WILDCARD 88
IC1A
CD74ACT00E

550

FIG.20B

* BYPASS ALL POWER SUPPLY LINES ON WBB AND DRAM
* WITH 10uF AND .1uF CAPS.
* BYPASS ALL ICS WITH .1uF MONOLYTHIC CAPS
* ANY STYLE OF RESISTORS MAY BE USED : DIP, SIP OR SINGLE
* THIS IS TO FACILITATE PCB LAYOUT



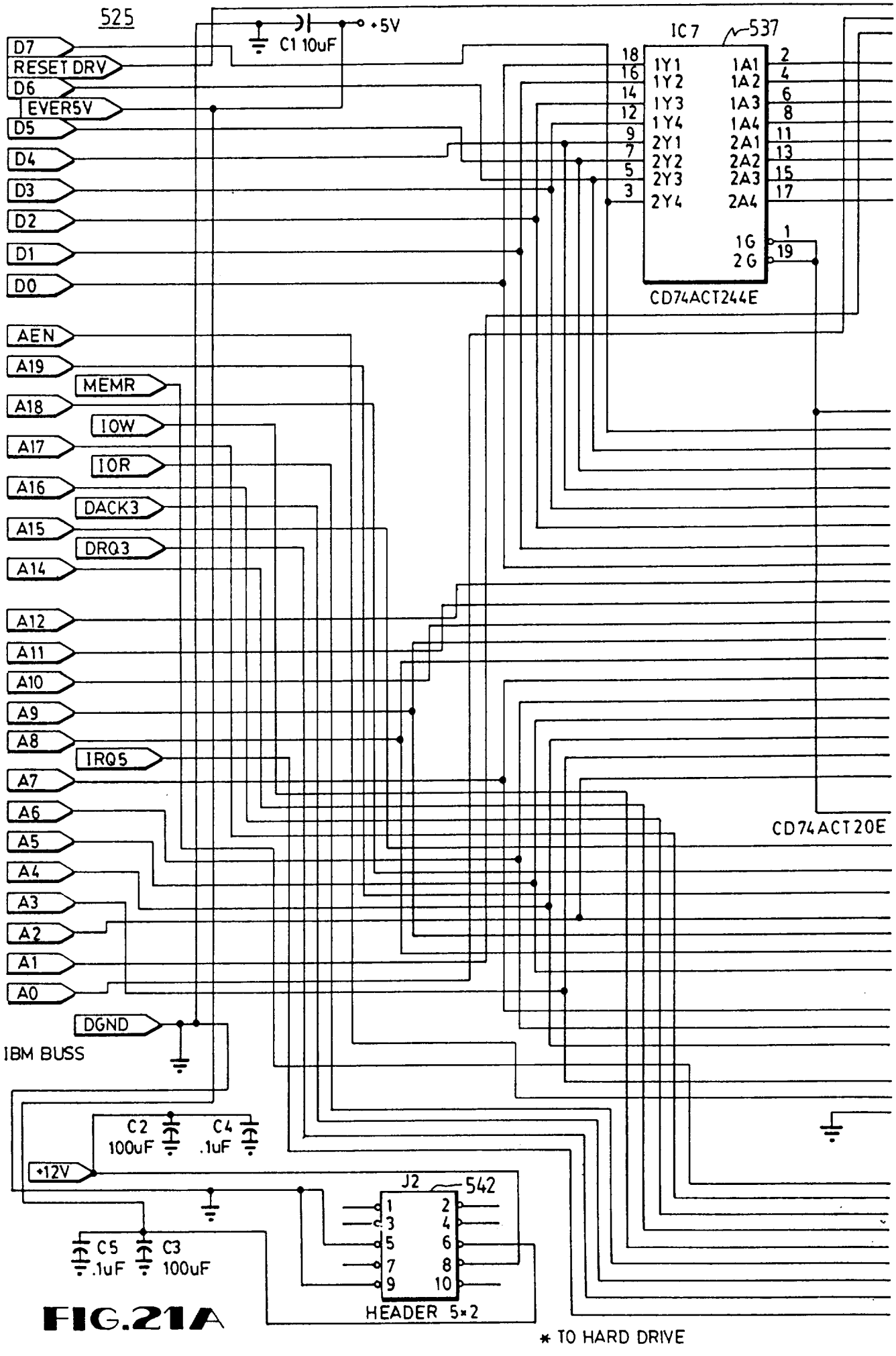

525
C1 10uF
+5V
IC7
537
CD74ACT244E
CD74ACT20E
D7
RESET DRV
D6
EVER5V
D5
D4
D3
D2
D1
D0
AEN
A19
A18
A17
A16
A15
A14
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
MEMR
IOW
IOR
DACK3
DRQ3
IRQ5
DGND
IBM BUSS
C2
100uF
C4
.1uF
+12V
C5
.1uF
C3
100uF
J2
542
HEADER 5×2
* TO HARD DRIVE

FIG.21A

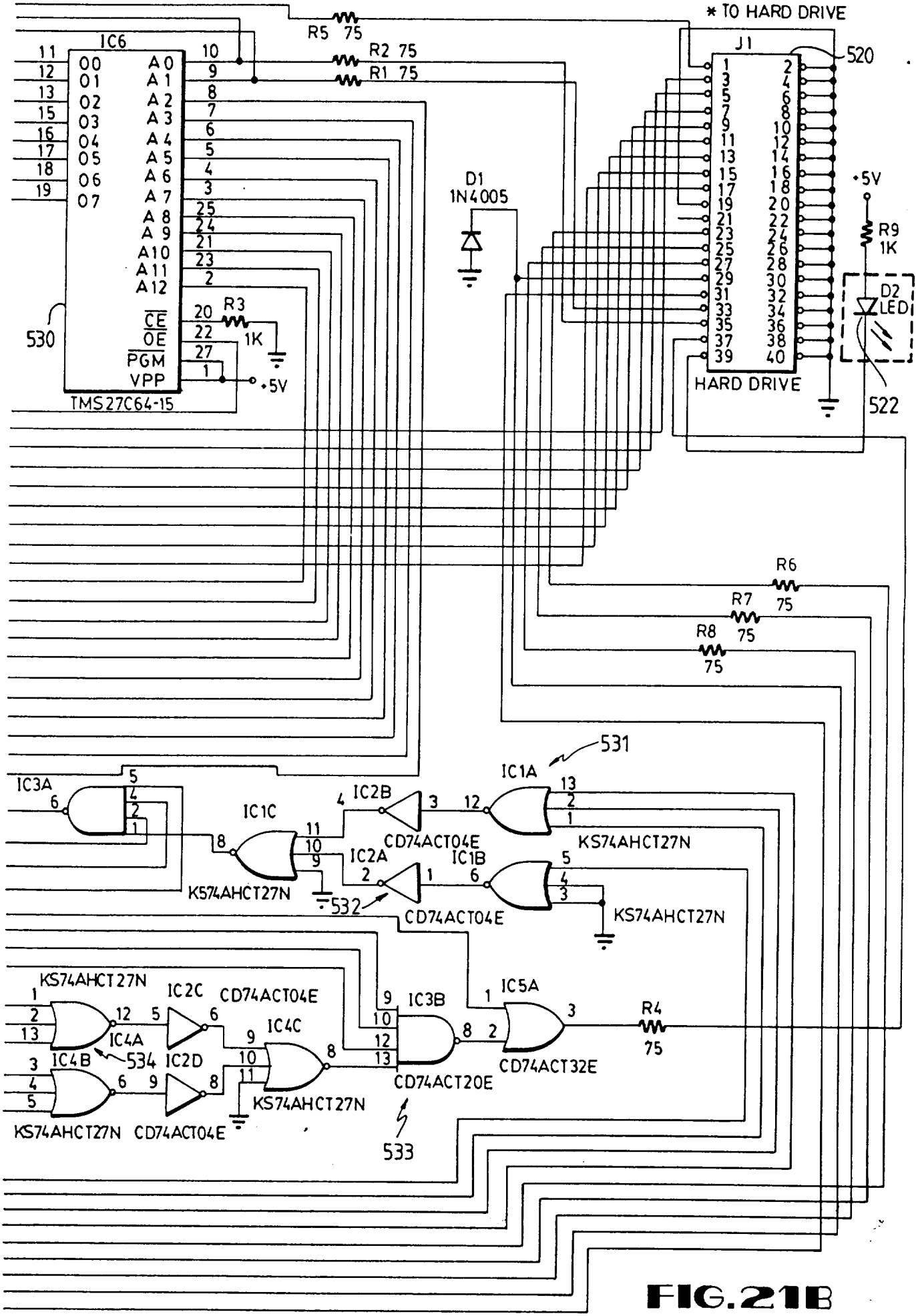
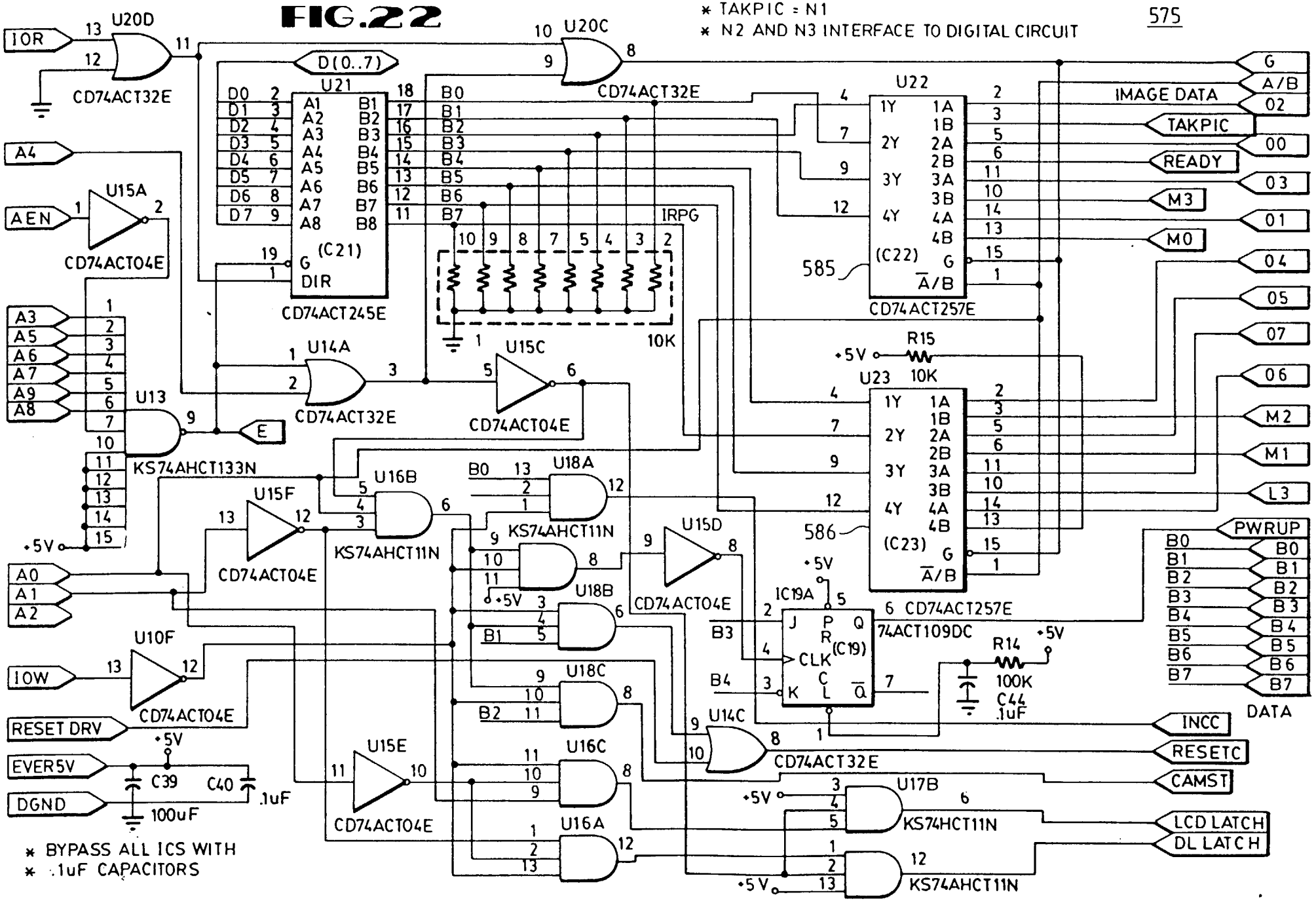


FIG.21B

* BYPASS ALL ICS WITH .1uF MONOLYTHIC CAP

FIG.22

* TAKPIC = N1
* N2 AND N3 INTERFACE TO DIGITAL CIRCUIT



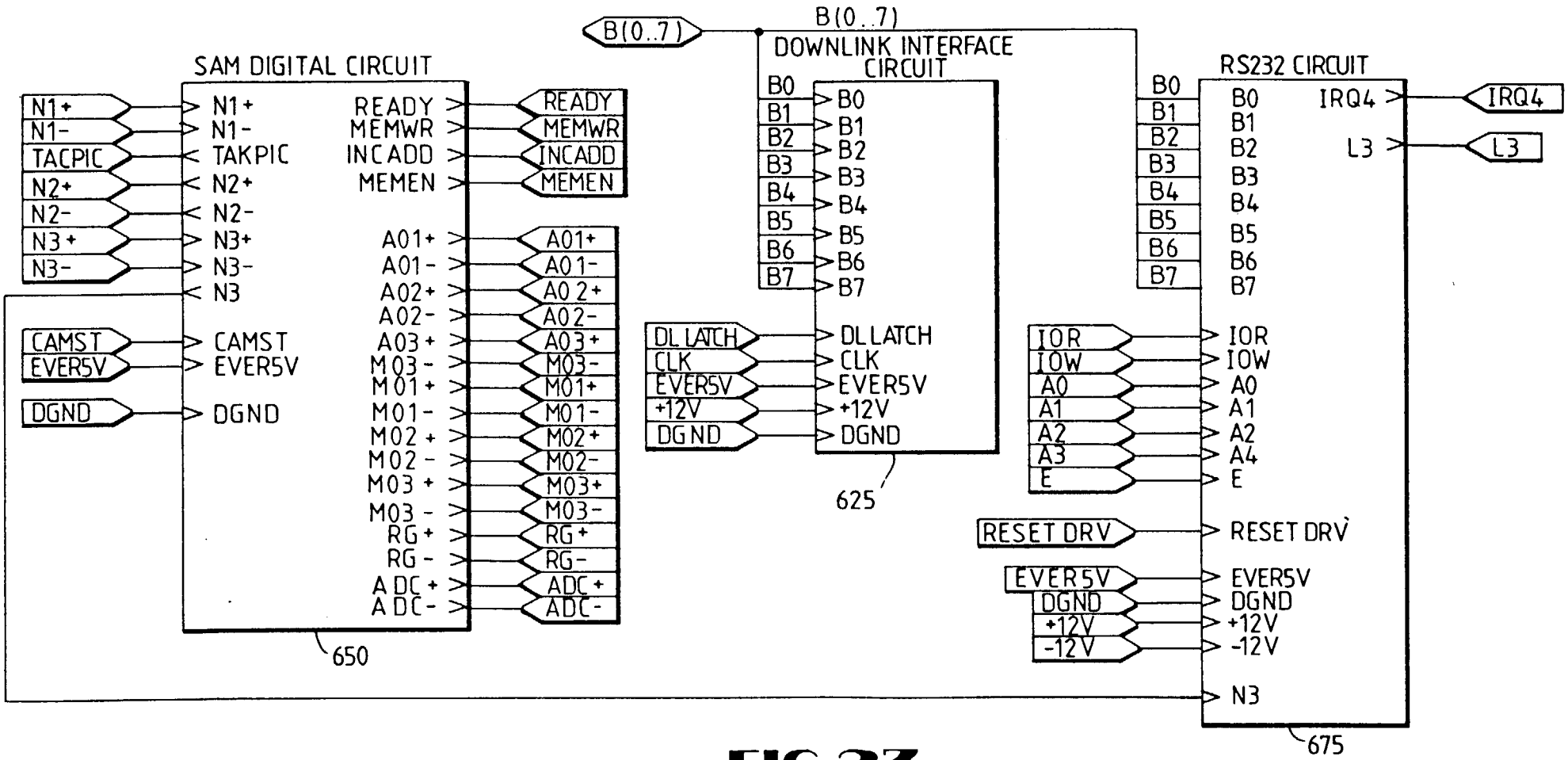

B(0..7)
B(0..7)
SAM DIGITAL CIRCUIT
DOWNLINK INTERFACE CIRCUIT
RS232 CIRCUIT
N1+
N1-
TACPIC
N2+
N2-
N3+
N3-
N3
CAMST
EVER5V
DGND
READY
MEMWR
INCADD
MEMEN
A01+
A01-
A02+
A02-
A03+
M03-
M01+
M01-
M02+
M02-
M03+
M03-
RG+
RG-
ADC+
ADC-
650
B0
B1
B2
B3
B4
B5
B6
B7
DL LATCH
CLK
EVER5V
+12V
DGND
625
IOR
IOW
A0
A1
A2
A3
E
RESET DRV
-12V
IRQ4
L3
A4
675

FIG.23

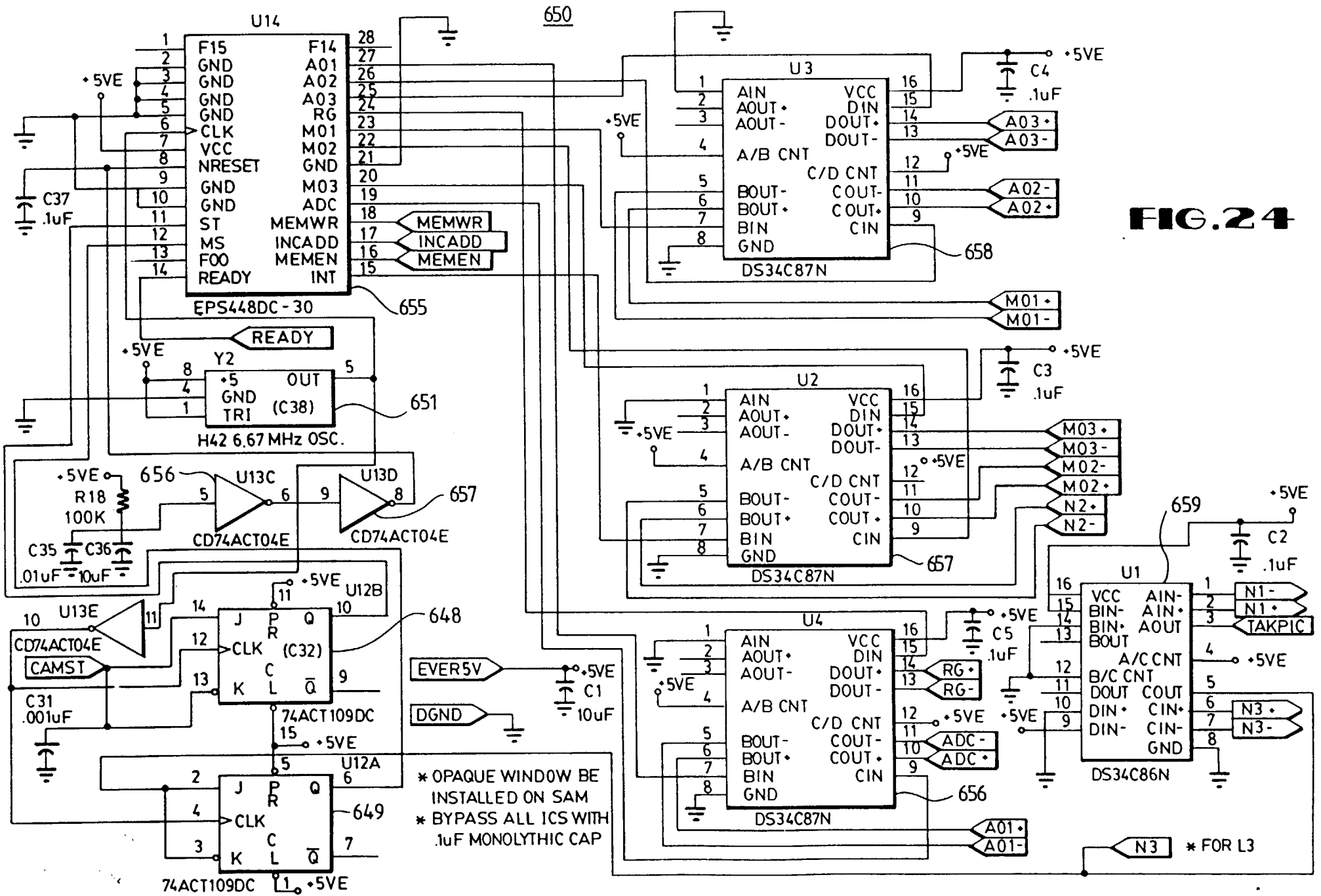

650
U14
F15
GND
GND
GND
GND
CLK
VCC
NRESET
GND
GND
ST
MS
F00
READY
F14
A01
A02
A03
RG
M01
M02
GND
M03
ADC
MEMWR
INCADD
MEMEN
INT
EPS448DC-30
655
+5VE
C37
.1uF
READY
Y2
+5
GND
TRI
OUT
(C38)
H42 6.67 MHz OSC.
651
R18
100K
C35
.01uF
C36
10uF
656
U13C
CD74ACT04E
U13D
CD74ACT04E
657
U13E
CD74ACT04E
CAMST
C31
.001uF
U12B
U12A
J
K
CLK
R
S
Q
(C32)
74ACT109DC
648
649
EVER5V
DGND
C1
10uF
* OPAQUE WINDOW BE INSTALLED ON SAM
* BYPASS ALL ICS WITH .1uF MONOLYTHIC CAP
U3
AIN
AOUT+
AOUT-
A/B CNT
BOUT-
BOUT+
BIN
GND
VCC
DIN
DOUT+
DOUT-
C/D CNT
COUT-
COUT+
CIN
DS34C87N
658
C4
.1uF
A03+
A03-
A02-
A02+
M01+
M01-
U2
DS34C87N
657
C3
.1uF
M03+
M03-
M02-
M02+
N2+
N2-
U4
DS34C87N
656
C5
.1uF
RG+
RG-
ADC-
ADC+
A01+
A01-
659
U1
VCC
BIN-
BIN+
BOUT
AIN-
AIN+
AOUT
A/C CNT
B/C CNT
DOUT
DIN+
DIN-
COUT
CIN+
CIN-
GND
DS34C86N
C2
.1uF
N1-
N1+
TAKPIC
N3+
N3-
N3
* FOR L3

FIG.24

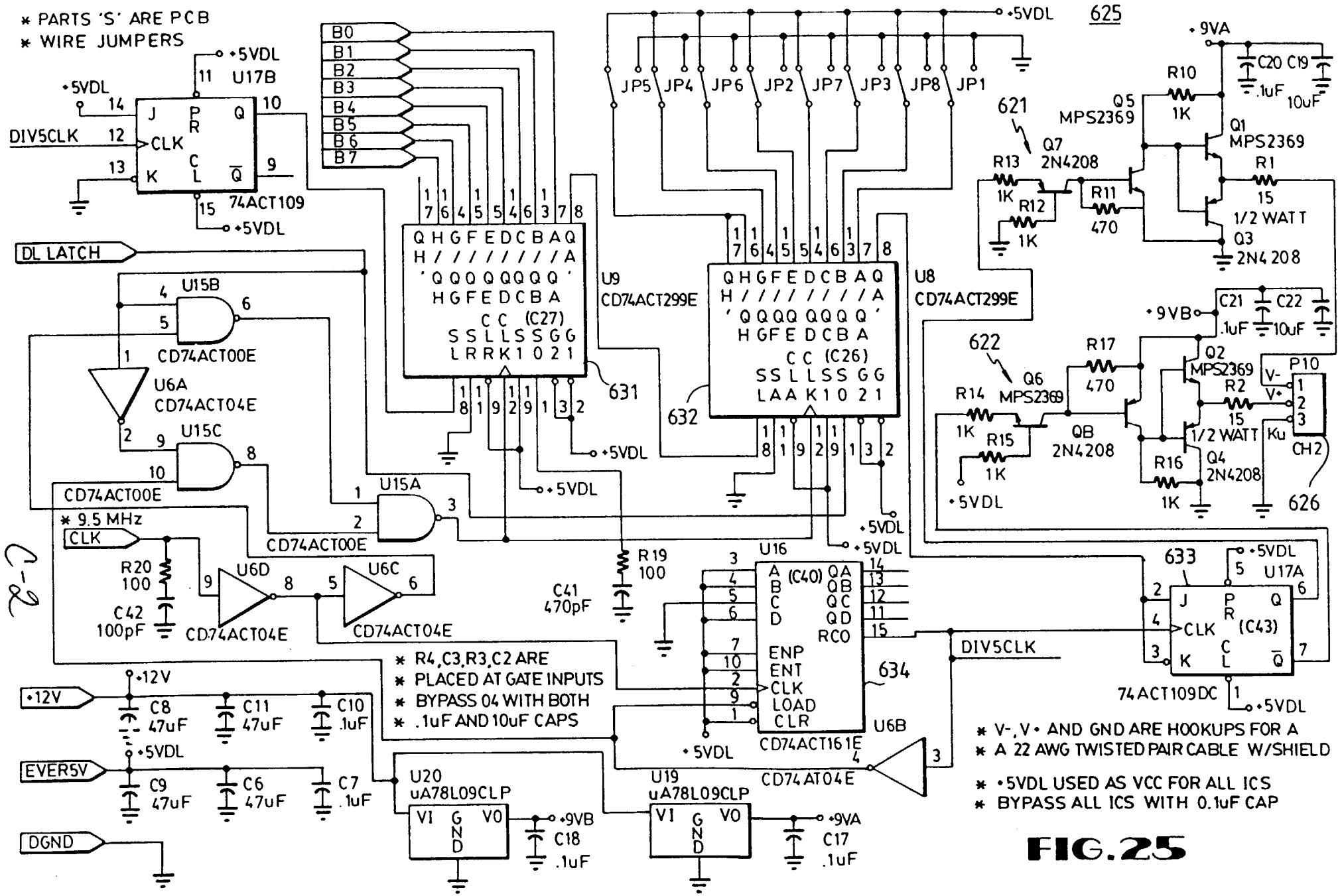
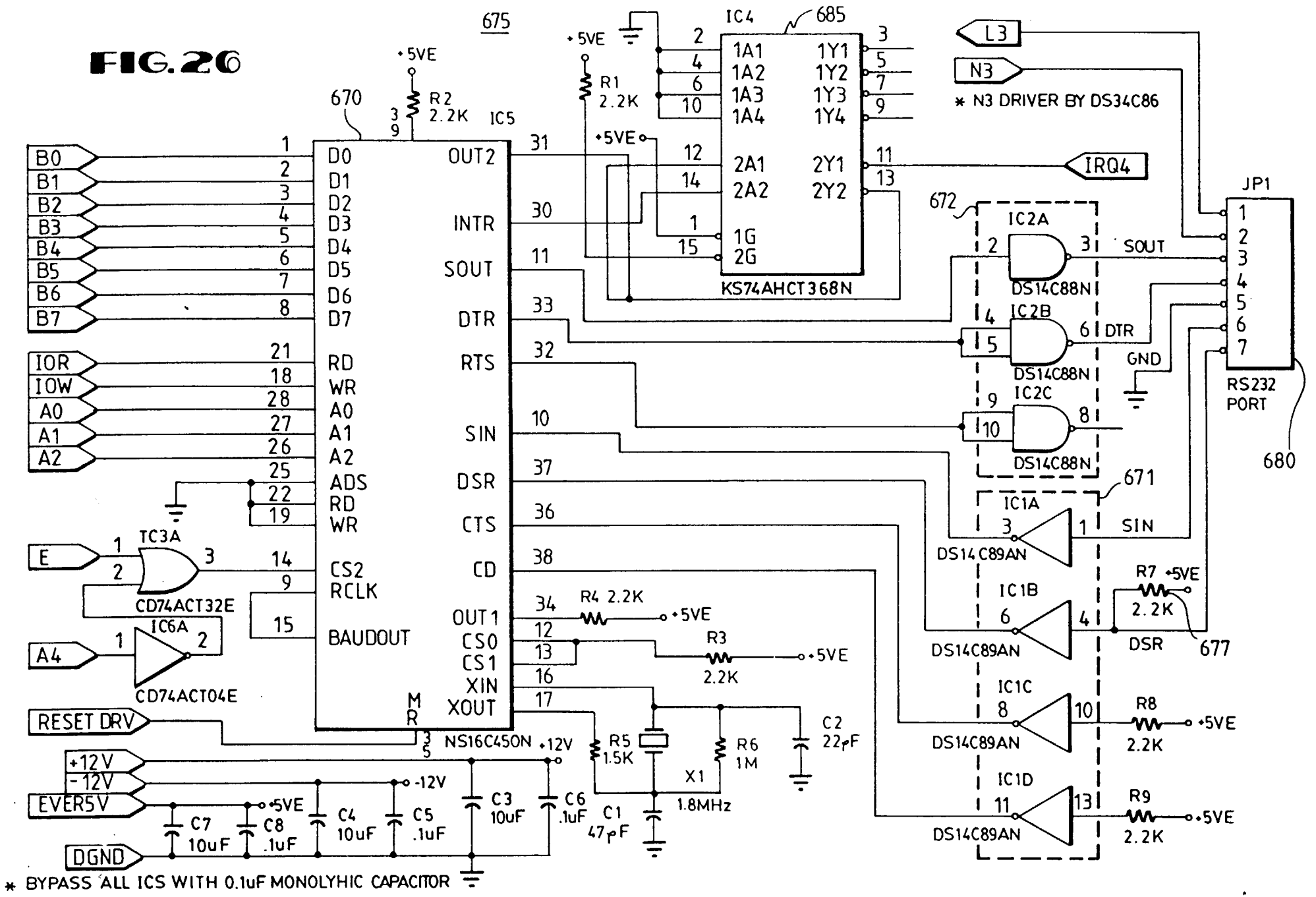

* PARTS 'S' ARE PCB
* WIRE JUMPERS
625
+5VDL
+9VA
U17B
74ACT109
DIV5CLK
B0
B1
B2
B3
B4
B5
B6
B7
JP5 JP4 JP6 JP2 JP7 JP3 JP8 JP1
621
Q5 MPS2369
Q7 2N4208
Q1 MPS2369
Q3 2N4208
R10 1K
R13 1K
R12 1K
R11 470
R1 15 1/2 WATT
C20 C19 .1uF 10uF
DL LATCH
U15B
CD74ACT00E
U6A CD74ACT04E
U15C
U15A
U9 CD74ACT299E
U8 CD74ACT299E
631
632
622
Q6 MPS2369
QB 2N4208
Q2 MPS2369
Q4 2N4208
R17 470
R14 1K
R15 1K
R16 1K
R2 15 1/2 WATT
+9VB
C21 .1uF
C22 10uF
P10
V-
V+
Ku
CH2
626
* 9.5 MHz
CLK
R20 100
C42 100pF
U6D
U6C
CD74ACT04E
R19 100
C41 470pF
U16
CD74ACT161E
633
U17A
74ACT109DC
DIV5CLK
634
U6B
CD74AT04E
* R4,C3,R3,C2 ARE
* PLACED AT GATE INPUTS
* BYPASS 04 WITH BOTH
* .1uF AND 10uF CAPS
* V-, V+ AND GND ARE HOOKUPS FOR A
* A 22 AWG TWISTED PAIR CABLE W/SHIELD
* +5VDL USED AS VCC FOR ALL ICS
* BYPASS ALL ICS WITH 0.1uF CAP
+12V
EVER5V
DGND
C8 47uF
C11 47uF
C10 .1uF
C9 47uF
C6 47uF
C7 .1uF
U20 uA78L09CLP
U19 uA78L09CLP
C18 .1uF
C17 .1uF
C-2

FIG.25

FIG.26


675
670
IC5
685
IC4
+5VE
R2 2.2K
R1 2.2K
B0
B1
B2
B3
B4
B5
B6
B7
D0
D1
D2
D3
D4
D5
D6
D7
IOR
IOW
A0
A1
A2
RD
WR
ADS
CS2
RCLK
BAUDOUT
OUT2
INTR
SOUT
DTR
RTS
SIN
DSR
CTS
CD
OUT1
CS0
CS1
XIN
XOUT
NS16C450N
1A1
1A2
1A3
1A4
2A1
2A2
1G
2G
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
KS74AHCT368N
L3
N3
* N3 DRIVER BY DS34C86
IRQ4
672
IC2A
IC2B
IC2C
DS14C88N
SOUT
DTR
GND
JP1
RS232 PORT
680
671
IC1A
IC1B
IC1C
IC1D
DS14C89AN
SIN
DSR
677
R7 2.2K
R8 2.2K
R9 2.2K
R4 2.2K
R3 2.2K
R5 1.5K
R6 1M
X1
1.8MHz
C1 47pF
C2 22pF
C3 10uF
C4 10uF
C5 .1uF
C6 .1uF
C7 10uF
C8 .1uF
E
TC3A
CD74ACT32E
A4
IC6A
CD74ACT04E
RESET DRV
+12V
-12V
EVER5V
DGND
* BYPASS ALL ICS WITH 0.1uF MONOLYHIC CAPACITOR

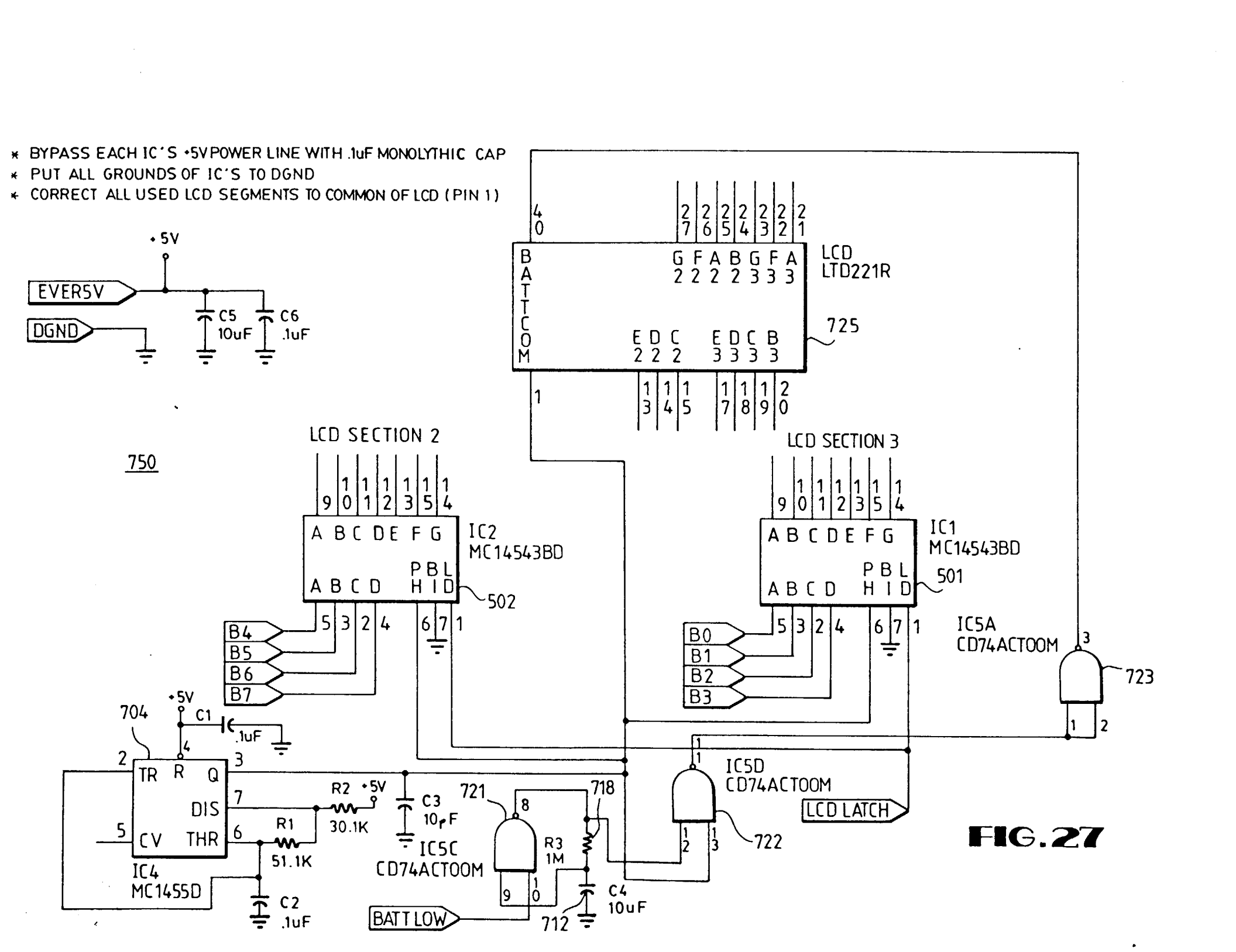

* BYPASS EACH IC'S +5V POWER LINE WITH .1uF MONOLYTHIC CAP
* PUT ALL GROUNDS OF IC'S TO DGND
* CORRECT ALL USED LCD SEGMENTS TO COMMON OF LCD (PIN 1)
+5V
EVER5V
DGND
C5
10uF
C6
.1uF
LCD
LTD221R
725
BATTCOM
LCD SECTION 2
LCD SECTION 3
750
IC2
MC14543BD
502
IC1
MC14543BD
501
IC5A
CD74ACTOOM
723
B4
B5
B6
B7
B0
B1
B2
B3
704
C1
.1uF
IC4
MC1455D
R1
51.1K
R2
30.1K
C3
10pF
IC5C
CD74ACTOOM
721
718
R3
1M
C4
10uF
712
BATT LOW
IC5D
CD74ACTOOM
722
LCD LATCH

FIG. 27

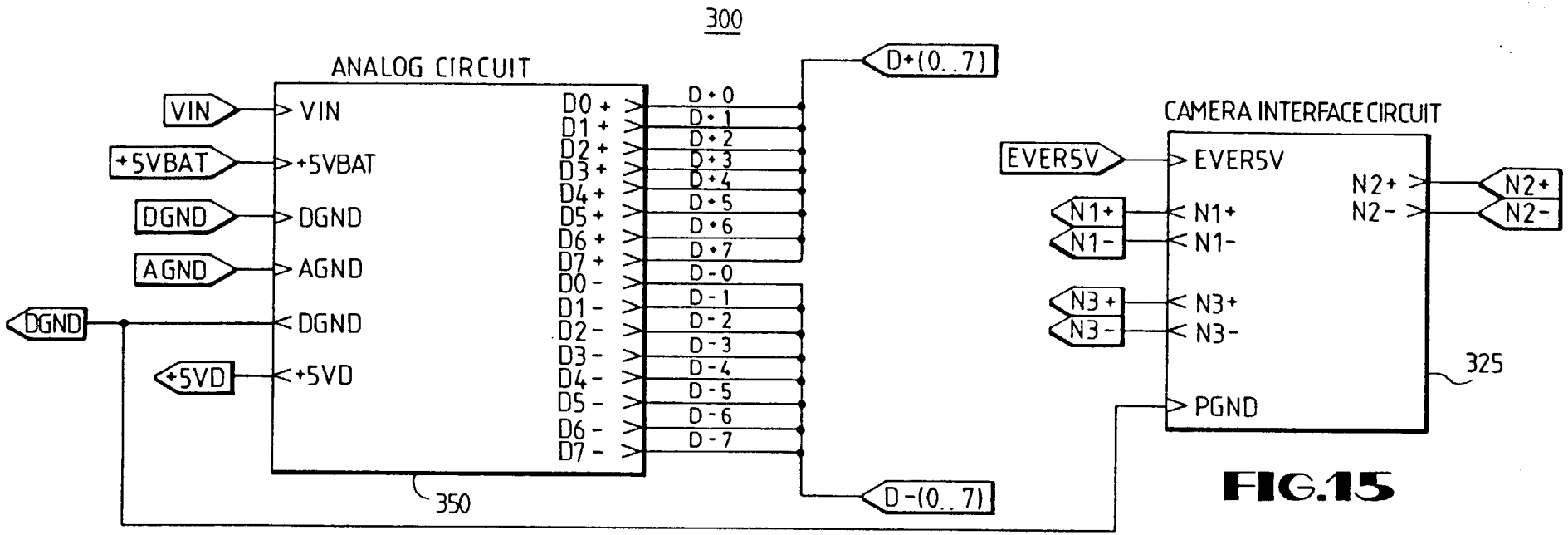

300
ANALOG CIRCUIT
VIN
+5VBAT
DGND
AGND
DGND
+5VD
D0+
D1+
D2+
D3+
D4+
D5+
D6+
D7+
D0-
D1-
D2-
D3-
D4-
D5-
D6-
D7-
D+0
D+1
D+2
D+3
D+4
D+5
D+6
D+7
D-0
D-1
D-2
D-3
D-4
D-5
D-6
D-7
D+(0..7)
D-(0..7)
350
CAMERA INTERFACE CIRCUIT
EVER5V
N1+
N1-
N3+
N3-
N2+
N2-
PGND
325

FIG.15

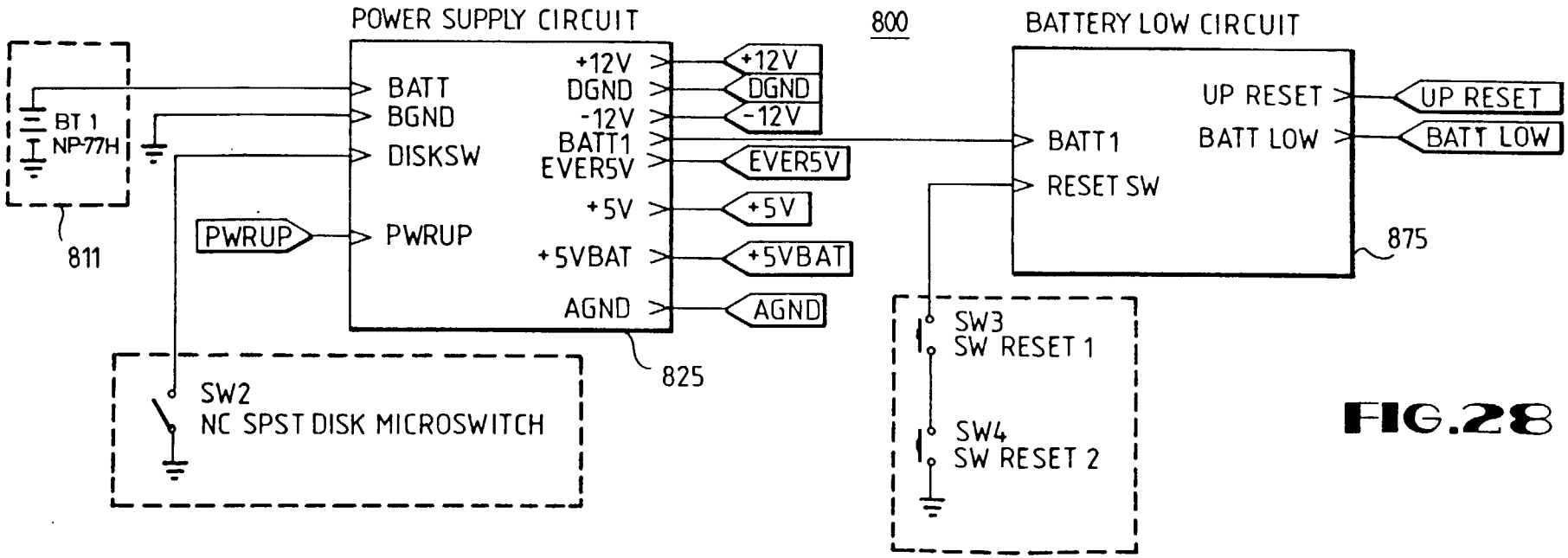

POWER SUPPLY CIRCUIT
800
BT 1
NP-77H
811
BATT
BGND
DISKSW
PWRUP
+12V
DGND
-12V
BATT1
EVER5V
+5V
+5VBAT
AGND
825
SW2
NC SPST DISK MICROSWITCH
BATTERY LOW CIRCUIT
BATT1
RESET SW
UP RESET
BATT LOW
875
SW3
SW RESET 1
SW4
SW RESET 2

FIG.28

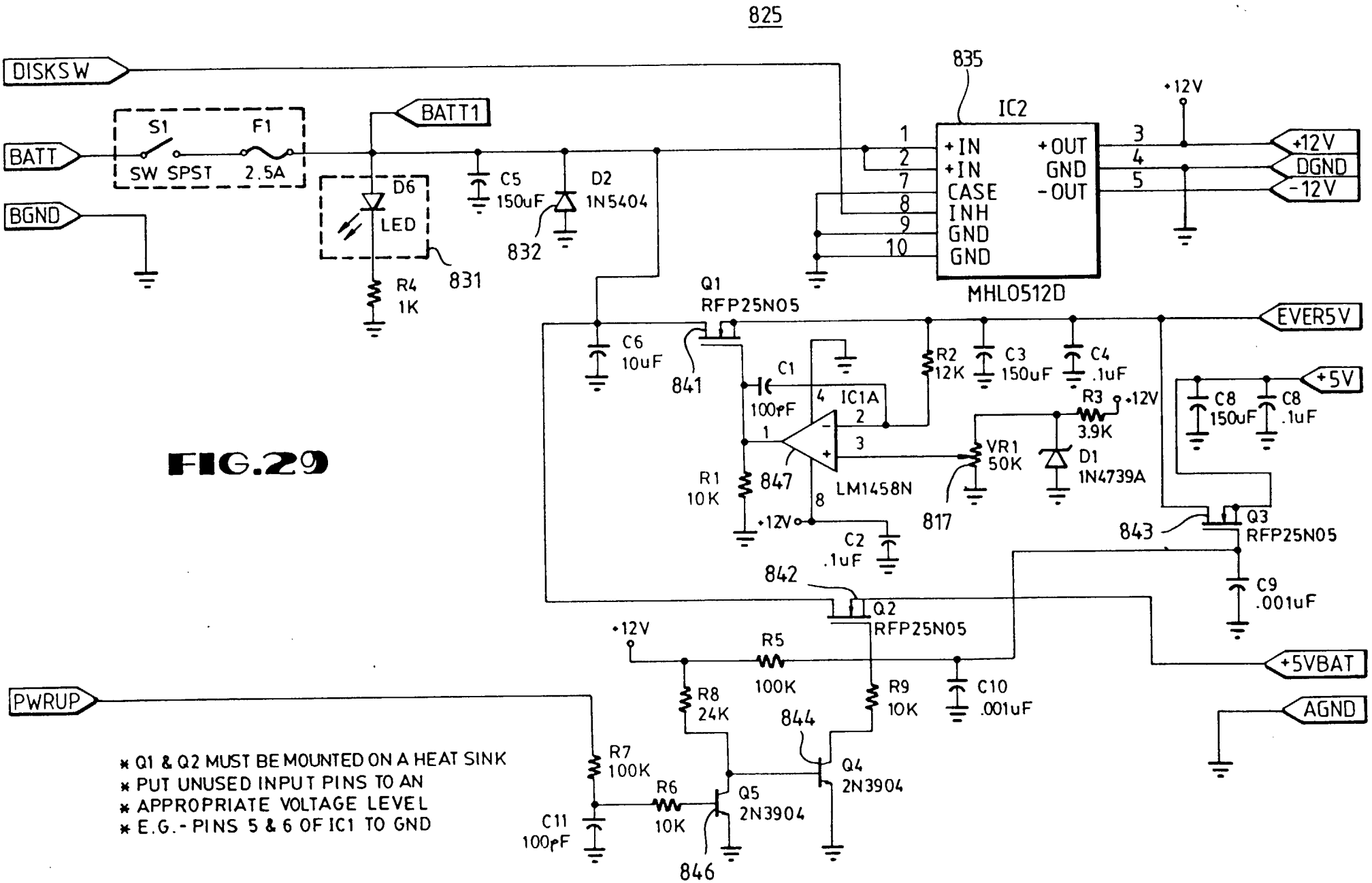

825
DISKSW
BATT
BGND
S1
F1
SW SPST
2.5A
BATT1
D6
LED
831
R4
1K
C5
150uF
D2
1N5404
832
835
IC2
+IN
+IN
CASE
INH
GND
GND
+OUT
GND
-OUT
MHL0512D
+12V
+12V
DGND
-12V
Q1
RFP25N05
841
C6
10uF
C1
100pF
IC1A
LM1458N
R1
10K
847
R2
12K
C3
150uF
C4
.1uF
R3
3.9K
VR1
50K
D1
1N4739A
817
C2
.1uF
EVER5V
+5V
C8
150uF
C8
.1uF
Q3
RFP25N05
843
C9
.001uF
842
Q2
RFP25N05
+5VBAT
AGND
R5
100K
R8
24K
R9
10K
C10
.001uF
844
Q4
2N3904
PWRUP
R7
100K
R6
10K
Q5
2N3904
C11
100pF
846
* Q1 & Q2 MUST BE MOUNTED ON A HEAT SINK
* PUT UNUSED INPUT PINS TO AN
* APPROPRIATE VOLTAGE LEVEL
* E.G.- PINS 5 & 6 OF IC1 TO GND

FIG.29

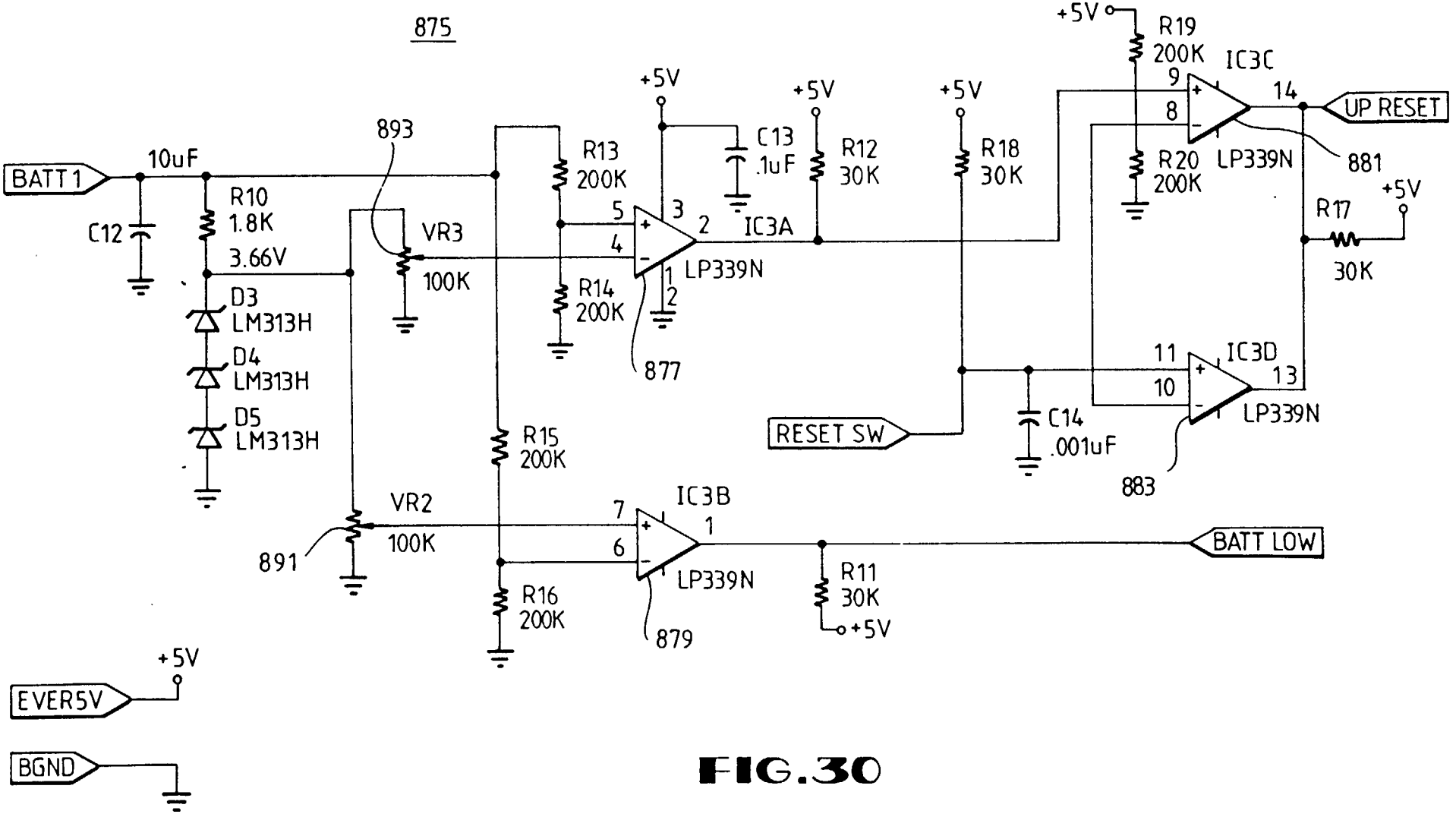
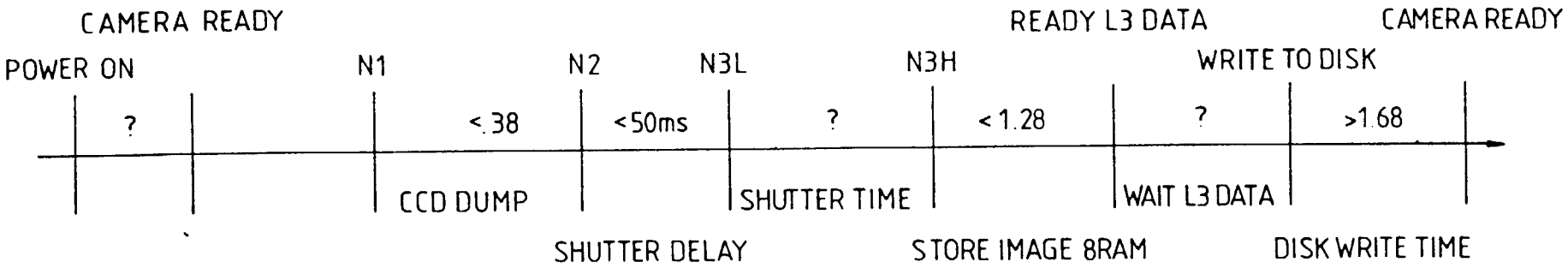

875
BATT 1
10uF
C12
R10
1.8K
3.66V
D3
LM313H
D4
LM313H
D5
LM313H
893
VR3
100K
R13
200K
R14
200K
+5V
C13
.1uF
IC3A
LP339N
877
+5V
R12
30K
+5V
R18
30K
+5V
R19
200K
IC3C
R20
200K
LP339N
881
UP RESET
+5V
R17
30K
RESET SW
C14
.001uF
IC3D
LP339N
883
R15
200K
VR2
100K
891
IC3B
LP339N
879
R16
200K
R11
30K
+5V
BATT LOW
+5V
EVER5V
BGND

FIG.30

CAMERA OPERATIONS TIME LINE



* NOTE - DISK WRITE TIME IS DISK DRIVE DEPENDENT
20 MBYTE = .625 MBYTES PER SECOND
42 8 MBYTES = 1.25 MBYTES PER SECOND

* NOTE - L3 WILL WAIT UP TO 16 SECONDS FOR ESC
ESC WILL WAIT INDEFINITELY FOR L3
ESC WAIT PERIOD CAN BE MODIFIED USING INTERRUPTS.

FIG.31

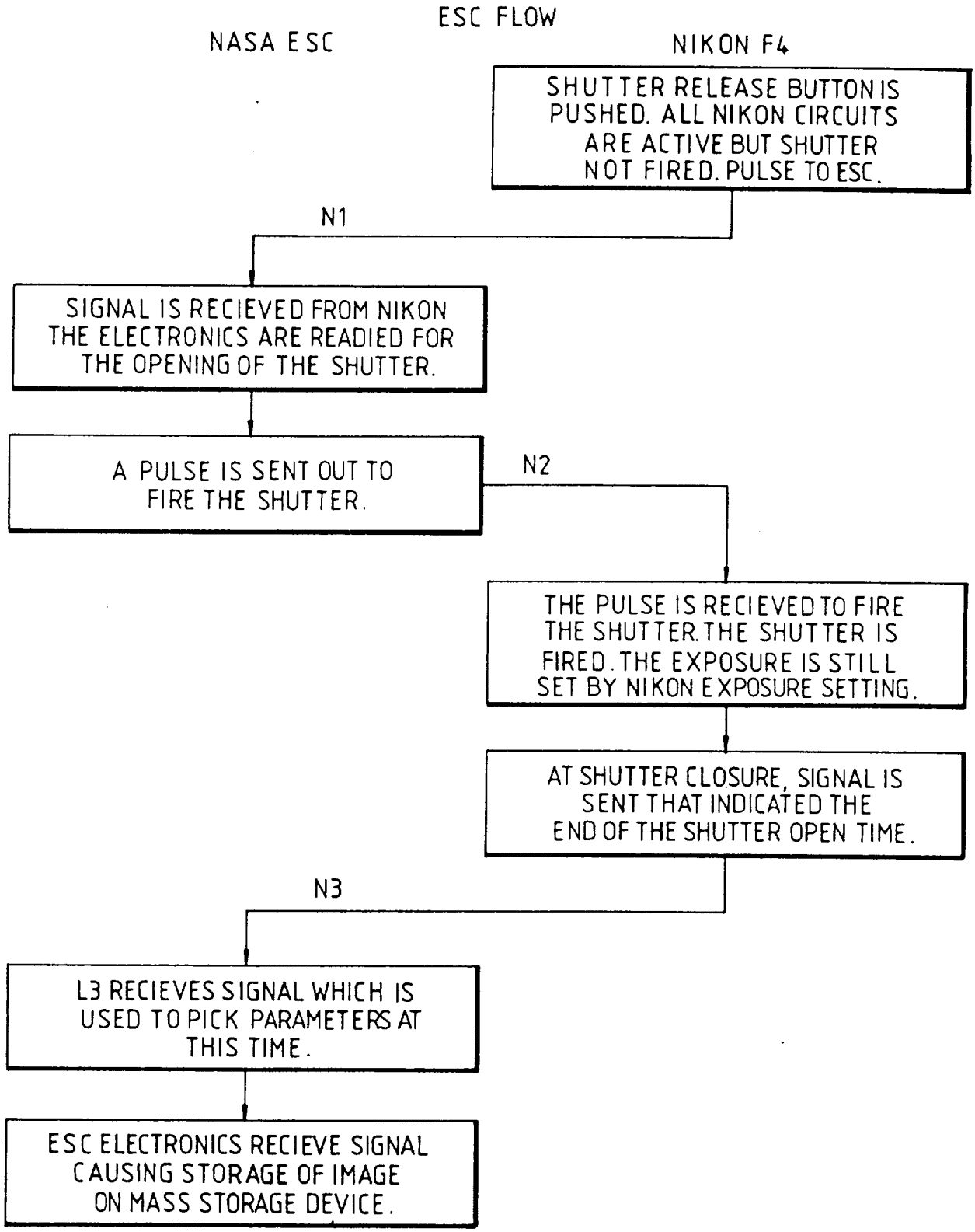

ESC FLOW
NASA ESC
NIKON F4
SHUTTER RELEASE BUTTON IS PUSHED. ALL NIKON CIRCUITS ARE ACTIVE BUT SHUTTER NOT FIRED. PULSE TO ESC.
N1
SIGNAL IS RECIEVED FROM NIKON THE ELECTRONICS ARE READIED FOR THE OPENING OF THE SHUTTER.
A PULSE IS SENT OUT TO FIRE THE SHUTTER.
N2
THE PULSE IS RECIEVED TO FIRE THE SHUTTER. THE SHUTTER IS FIRED. THE EXPOSURE IS STILL SET BY NIKON EXPOSURE SETTING.
AT SHUTTER CLOSURE, SIGNAL IS SENT THAT INDICATED THE END OF THE SHUTTER OPEN TIME.
N3
L3 RECIEVES SIGNAL WHICH IS USED TO PICK PARAMETERS AT THIS TIME.
ESC ELECTRONICS RECIEVE SIGNAL CAUSING STORAGE OF IMAGE ON MASS STORAGE DEVICE.

FIG.32